Figure 6.1 Basic structure of an n-channel MOSFET.
Figure 6.2 (a) Typical biases applied to the n-channel MOSFET ($V_{GS} > V_I$). (b) Simplified circuit symbol with the same biases.
Figure 6.3 Ideal current-voltage characteristics of n-channel MOSFET assuming $V_T = 0.5$ V.
Figure 6.4 (a) A circuit that can amplify a time-varying input signal $v_i$. (b) Load line and time-varying signals superimposed on transistor characteristics.
(a) accumulation

(b) depletion and weak inversion
Figure 6.9 Energy bands in the p-type semiconductor and charge distribution on the metal and in the semiconductor for (a) $V_G < 0$ (accumulation), (b) $V_G > 0$; (c) $V_G = V_T$ (threshold), and (d) $V_G > V_T$ (inversion).
Figure 6.10 The MOS capacitor with an n-type substrate for (a) a positive gate bias, showing an accumulation layer of electrons adjacent to the semiconductor-oxide interface, and (b) a moderate negative gate bias, showing an induced positive space charge region in the semiconductor.
NFET: p substrate

- Accumulation: \( \phi_s < 0 \ p_s > p_o \ V_g < V_{FB} \)

- Flat band (no charge transfer, Vox?0): \( \phi_s = 0, \ p_s = p_o \ V_g = V_{FB} \)

- Depletion: \( 0 < \phi_s < \phi_{Fp} \ (ns < ps) < po = NA \ V_g > V_{FB} \)

- Weak inversion: \( \phi_{Fp} < \phi_s < 2\phi_{Fp} \ ns > ps \ V_g >> V_{FB} \)

- OFF depletion \( x_d = \left( \frac{2\varepsilon_s \phi_s}{eN_a} \right)^{1/2} \) \( (6.9) \)

- Strong inversion: \( \phi_s < 2\phi_{Fp} \ n_s > p_o \ V_g > V_T \)

ON

\[ x_{dT} = \left( \frac{4\varepsilon_s \phi_{Fp}}{eN_a} \right)^{1/2} \] \( (6.12) \)
Figure 6.13 Energy-band diagram in the p-type semiconductor, showing the potential \( \phi_{FP} \) and the surface potential \( \phi_s \).

\[
\phi_{FP} = -V_i \ln \left( \frac{N_a}{n_i} \right) \quad (6.8b)
\]

\[
x_d = \left( \frac{2 \varepsilon_s \phi_s}{eN_a} \right)^{1/2} \quad (6.9)
\]

\[
x_{dT} = \left( \frac{4 \varepsilon_s |\phi_{FP}|}{eN_a} \right)^{1/2} \quad (6.12)
\]
\[ V_{FB} = \phi_{ms} = \left[ \phi'_m - \left( \chi' + \frac{E_g}{2e} + |\phi_{FP}| \right) \right] \]

(6.18)
Battery concept

\[ V_{FB} = e\phi'_m - e\phi'_s = -(E_{Fm} - E_F) / e \]
Figure 6.18 (a) Energy levels in an MOS system prior to contact and (b) energy-band diagram through the MOS structure in thermal equilibrium after contact. Another interpretation: the internal potential drop at zero applied bias.

\[
\phi_{ms} = \left[ \phi_m' - \left( \chi' + \frac{E_g}{2e} + |\phi_{Fp}| \right) \right]
\]  (6.18)
\[ V_{FB} = e\phi_m' - e\phi_s' = -(E_{Fm} - E_F) / e \]

Figure 6.31 Energy-band diagram through the MOS structure at flat-band with \( Q'_{ss} = 0 \).

\[ \phi_{ms} = \left[ \phi_m' - \left( \chi' + \frac{E_g}{2e} + |\phi_{Fp}| \right) \right] \hspace{2cm} (6.18) \text{ work function difference between metal and Si} \]
Figure 6.19 Energy-band diagram through the MOS structure with a p-type substrate at zero bias for (a) an n⁺ polysilicon gate and (b) a p⁺ polysilicon gate. In the heavily doped polysilicon gates, the Fermi level is assumed to correspond to the conduction- and valence-band energies, respectively.
\[ \phi_{ms} = \left[ \chi' - \left( \chi' + \frac{E_g}{2e} + |\phi_{Fp}| \right) \right] = -\left( \frac{E_g}{2e} + |\phi_{Fp}| \right) \] (6.19) n+ poly gate

\[ \phi_{ms} = \left[ \left( \chi' + \frac{E_g}{e} \right) - \left( \chi' + \frac{E_g}{2e} + |\phi_{Fp}| \right) \right] = \left( \frac{E_g}{2e} - |\phi_{Fp}| \right) \] (6.20) p+ poly gate
Figure 6.32 Energy-band diagram through the MOS structure at flat-band with $Q'_{ss} > 0$.

$$V_G = V_{FB} = \phi_{ms} - \frac{Q'_{ss}}{C_{ox}}$$  \hspace{1cm} (6.28)
Figure 6.22 MOS structure showing equivalent fixed positive charge $Q'_ss$ in oxide adjacent to the semiconductor-oxide interface. Also shown is the interface trapped charge.

$Q'_{ss}$: equivalent oxide charge at interface

\[ V_G = V_{FB} = \phi_{ms} - \frac{Q'_{ss}}{C_{ox}} \]  

(6.28)

1. fixed charge
2. Oxide trap charge
3. Mobile charge: Na
4. Interface trap charge Dit or Qit

169
Figure 6.26 Energy-band diagram through the MOS structure with a positive applied gate bias.

\[
\begin{align*}
|Q'_{SD}(\text{max})| &= eN_a x_{dT} \\
V_{TN} &= V_{FB} + 2|\phi_F| + \frac{|Q'_{SD}(\text{max})|}{C_{ox}} \\
&= V_{FB} + V_{\text{ox}} = \frac{eN_a \varepsilon_{sp} \phi_p}{C_{ox}} + V_{\text{si}} = \phi_s \\
V_{TN} &= \left(\left|Q'_{SD}(\text{max}) - Q'_{ss}\right| - \frac{t_{ox}}{\varepsilon_{ox}}\right) + \phi_m + 2|\phi_F| \\
V_G &= V_{TN} \\
\text{where } \phi_s &= 2|\phi_F| 
\end{align*}
\]
Figure 6.33 (a) Energy-band diagram through the MOS structure for $V_G > V_T$. (b) Charge distribution and electric field profile through the MOS capacitor for $V_G > V_T$. As an approximation, the inversion charge density is assumed to be a constant over a finite distance.
Figure 6.34 (a) Energy-band diagram through an MOS capacitor for the accumulation mode. (b) Differential charge distribution at accumulation for a differential change in gate voltage.

\[ C'(\text{acc}) = C_{\text{ox}} = \frac{\varepsilon_{\text{ox}}}{t_{\text{ox}}} \quad (6.40) \]
Figure 6.35 (a) Energy-band diagram through an MOS capacitor for the depletion mode. (b) Differential charge distribution at depletion for a differential change in gate voltage.

\[ C'(\text{depl}) = \frac{C_{ox}}{1 + \frac{C_{ox}}{C'_{SD}}} = \frac{\varepsilon_{ox}}{t_{ox} + \left(\frac{\varepsilon_{ox}}{\varepsilon_{s}}\right)x_d} \]  

(6.42)
Figure 6.36 (a) Energy-band diagram through an MOS capacitor for the inversion mode. (b) Differential charge distribution at inversion for a low-frequency differential change in gate voltage.

\[ C'_{\text{inv}} = C_{\text{ox}} = \frac{\varepsilon_{\text{ox}}}{t_{\text{ox}}} \quad (6.44) \]
Figure 6.37 Ideal low-frequency capacitance versus gate voltage of an MOS capacitor with a p-type substrate. Simplified ideal capacitance curve is shown by the dotted line.

\[ C'_{FB} = \frac{\varepsilon_{ox}}{t_{ox} + \left( \frac{\varepsilon_{ox}}{\varepsilon_{s}} \right) \left( \frac{kT}{e} \right) \left( \frac{\varepsilon_{s}}{eN_{a}} \right)} \]

\[ (6.45) \]
LF C-V curves of a p-si MOS capacitor

\[ C \cong C_{OX} \]

\[ C = \frac{|V_g - \Psi_s|}{|V_g - \Psi_s| + \frac{2kT}{q}} \cdot C_{ox} (\psi_s : 0.1 \sim 0.3V) \]

\[ C = \frac{|V_g - \Psi_s|}{|V_g - \Psi_s| + \frac{2kT}{q}} \cdot C_{ax} (\psi_s : 0.7 \sim 1V) \]

\[ C = \frac{C_{sd} \cdot C_{ox}}{C_{sd} + C_{ox}} = \frac{C_{ox}}{\sqrt{1 + \left( \frac{2C_{ox}V_g}{\varepsilon_s q N_a} \right)}} \]
Figure 6.39 Differential charge distribution at inversion for a high-frequency differential change in gate voltage.

\[ C'_{\text{min}} = \frac{\varepsilon_{\text{ox}}}{t_{\text{ox}} + \left( \frac{\varepsilon_{\text{ox}}}{\varepsilon_s} \right) x_{dT}} \]  

(6.43)
Figure 6.40 Low-frequency and high-frequency capacitance versus gate voltage of an MOS capacitor with a p-type substrate.
Figure 6.41 High-frequency capacitance versus gate voltage of an MOS capacitor with a p-type substrate for several values of effective trapped oxide charge.

\[ V_{FB} = \phi_{mS} - \frac{Q_{ss}'}{C_{ox}} \]
Figure 6.42 Schematic diagram showing interface states at the oxide-semiconductor interface.
Figure 6.43 Energy-band diagram in a p-type semiconductor showing the charge trapped in the interface states when the MOS capacitor is biased (a) in accumulation, (b) at midgap, (c) at inversion.
Voltage Shifts Due to Interface Traps

Suppose $Q_{it}$ is Interface Trapped Charge, then

$$\Delta V_{fb} = - \frac{Q_{it} (@flatband)}{Cox}$$

$$\Delta V_{th} = - \frac{Q_{it} (@inversion)}{Cox}$$

**Experimental Observation:**

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<th>P-channel FET</th>
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<td>$\Delta V_{th}$</td>
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Figure 6.44 High-frequency $C-V$ characteristics of an MOS capacitor showing effects of interface states.
(a) Channel inversion charge

(b) Channel inversion charge

$V_{GS1} > V_T$

Oxide

Depletion region

S

L

$V_{DS}$

$I_D$

$p$ type

$V_{DS(sat)}$

$V_{DS}$

$I_D$
Figure 6.50 Cross section and $I_D$ versus $V_{DS}$ curve when $V_{GS} < V_T$ for (a) a small $V_{DS}$ value, (b) a larger $V_{DS}$ value, (c) a value of $V_{DS} = V_{DS}(sat)$, and (d) a value of $V_{DS} > V_{DS}(sat)$. 185
\[ I = J \cdot \text{area} \quad J = qnv \quad n \propto C_{ox}(V_{gs} - V_t) \]

\[ v = \mu E \]

\[ \Rightarrow \quad C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \]

\[ I \propto \frac{1}{2} \mu C_{ox} \frac{W}{L} (V_{gs} - V_t)^{\alpha} \]

Q2D = (Q(S) + Q(D)) / 2

High K \Rightarrow n \uparrow \Rightarrow \text{strained Si} \Rightarrow v(\mu) \uparrow

Driving current \uparrow \Rightarrow \text{Device speed} \uparrow
Figure 6.51 Family of $I_D$ versus $V_{DS}$ curves for an n-channel enhancement-mode MOSFET.

$$I_D = K_n \left[ 2(V_{GS} - V_{TN})V_{DS} - V_{DS}^2 \right]$$  \hspace{1cm} (6.55)

Kn = $1/2 \ \text{un}C_{ox} \ W/L$
Figure 6. 55 (a) $I_D$ versus $V_{GS}$ (for small $V_{DS}$) for enhancement mode MOSFET. (b) Ideal $\sqrt{I_D}$ versus $V_{GS}$ in saturation region for enhancement mode (curve $A$) and depletion mode (curve $B$) n-channel MOSFETs.

\[
\sqrt{I_D} \text{(sat)} = \sqrt{\frac{W \mu_n C_{ox}}{2L}} (V_{GS} - V_{TN})
\]  

(6.59)
Figure 6.63 (a) Applied voltages on an n-channel MOSFET. (b) Energy-band diagram at inversion point when $V_{SB} = 0$. (c) Energy-band diagram at inversion point when $V_{SB} > 0$ is applied.

\[ e\phi_s = e(2|\phi_{FP}| + V_{SB}) \]

\[ \Delta V_T = \frac{-\Delta Q'_{SD}}{C_{ox}} = \frac{\sqrt{2e\varepsilon_s N_a}}{C_{ox}} \left[ \sqrt{2|\phi_{FP}| + V_{SB}} - \sqrt{2|\phi_{FP}|} \right] \]
Figure 6.64 Plots of $\sqrt{I_D}$ versus $V_{GS}$ at several values of $V_{SB}$ for an n-channel MOSFET.
Figure 6.65 Inherent resistances and capacitances in the n-channel MOSFET structure.
Figure 6.66 Small-signal equivalent circuit of a common-source n-channel MOSFET.
Figure 6.70 Small-signal equivalent circuit including Miller capacitance.

\[
f_T = \frac{g_m}{2\pi \left(C_{gs} + C_M\right)} = \frac{g_m}{2\pi C_G} \quad (6.102)
\]

\[
f_T = \frac{g_m}{2\pi C_G} = \frac{W\mu_n C_{ox}}{L} \left(V_{GS} - V_{TN}\right) = \frac{\mu_n (V_{GS} - V_{TN})}{2\pi L^2} \quad (6.103)
\]
Intrinsic MOSFET Capacitance

- Subthreshold region:
  \[ C_g = W L \left( \frac{1}{C_{ox}} + \frac{1}{C_d} \right)^{-1} \approx W L C_d \]

- Linear region:
  \[ C_g = W L C_{ox} \]

- Saturation region:
  \[ Q_i(y) = -C_{ox} \left( V_g - V_f \right) \sqrt{1 - \frac{y}{L}} \]
  \[ \Rightarrow C_g = \frac{2}{3} W L C_{ox} \]
\[ I_i = j\omega C_{gsT} V_{gs} + j\omega C_{gdT} (V_{gs} - V_d) \quad (6.94) \]

\[ \frac{V_d}{R_L} + g_m V_{gs} + j\omega C_{gdT} (V_d - V_{gs}) = 0 \quad (6.95) \]

\[ I_i = j\omega \left[ C_{gsT} + C_{gdT} \left( \frac{1 + g_m R_L}{1 + j\omega R_L C_{gdT}} \right) \right] V_{gs} \quad (6.96) \]

\[ I_i = j\omega \left[ C_{gsT} + C_{gdT} (1 + g_m R_L) \right] V_{gs} \quad (6.97) \]

\[ C_M = C_{gdT} (1 + g_m R_L) \quad (6.98) \]

\[ I_i = j\omega \left( C_{gsT} + C_M \right) V_{gs} \quad (6.99) \]

\[ I_d = g_m V_{gs} \quad (6.100) \]

\[ \frac{|I_d|}{|I_i|} = \frac{g_m}{2\pi f \left( C_{gsT} + C_M \right)} \quad (6.101) \]
Φs vs Vg relation (graduate school)

Simple idea
Metal gate tox=3nm, N=1E18
Band Diagram of High-K

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Si Eg = 1.12 eV