Chapter 4
Wafer Manufacturing and Epitaxy Growing

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Objectives

• Give two reasons why silicon dominate
• List at least two wafer orientations
• List the basic steps from sand to wafer
• Describe the CZ and FZ methods
• Explain the purpose of epitaxial silicon
• Describe the epi-silicon deposition process.
Crystal Structures

- Amorphous
  - No repeated structure at all
- Polycrystalline
  - Some repeated structures
- Single crystal
  - One repeated structure
Amorphous Structure
Polycrystalline Structure

Grain Boundary

Grain
Single Crystal Structure
Why Silicon?

• Abundant, cheap
• Silicon dioxide is very stable, strong dielectric, and it is easy to grow in thermal process.
• Large band gap, wide operation temperature range.
<table>
<thead>
<tr>
<th><strong>Name</strong></th>
<th><strong>Silicon</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Symbol</strong></td>
<td>Si</td>
</tr>
<tr>
<td><strong>Atomic number</strong></td>
<td>14</td>
</tr>
<tr>
<td><strong>Atomic weight</strong></td>
<td>28.0855</td>
</tr>
<tr>
<td><strong>Discoverer</strong></td>
<td>Jöns Jacob Berzelius</td>
</tr>
<tr>
<td><strong>Discovered at</strong></td>
<td>Sweden</td>
</tr>
<tr>
<td><strong>Discovery date</strong></td>
<td>1824</td>
</tr>
<tr>
<td><strong>Origin of name</strong></td>
<td>From the Latin word &quot;silicis&quot; meaning &quot;flint&quot;</td>
</tr>
<tr>
<td><strong>Bond length in single crystal Si</strong></td>
<td>2.352 Å</td>
</tr>
<tr>
<td><strong>Density of solid</strong></td>
<td>2.33 g/cm³</td>
</tr>
<tr>
<td><strong>Molar volume</strong></td>
<td>12.06 cm³</td>
</tr>
<tr>
<td><strong>Velocity of sound</strong></td>
<td>2200 m/sec</td>
</tr>
<tr>
<td><strong>Electrical resistivity</strong></td>
<td>100,000 μΩ⋅cm</td>
</tr>
<tr>
<td><strong>Reflectivity</strong></td>
<td>28%</td>
</tr>
<tr>
<td><strong>Melting point</strong></td>
<td>1414 °C</td>
</tr>
<tr>
<td><strong>Boiling point</strong></td>
<td>2900 °C</td>
</tr>
</tbody>
</table>

Source: [http://www.shef.ac.uk/chemistry/web-elements/nofr-key/Si.html](http://www.shef.ac.uk/chemistry/web-elements/nofr-key/Si.html)
Unit Cell of Single Crystal Silicon
Crystal Orientations: $\langle 100 \rangle$

$\langle 100 \rangle$ plane
Crystal Orientations: <111>
Crystal Orientations: $<110>$
<100> Orientation Plane

Basic lattice cell

Atom
<111> Orientation Plane

Basic lattice cell

Silicon atom
<100> Wafer Etch Pits
<111> Wafer Etch Pits
Illustration of the Defects

- Impurity on substitutional site
- Silicon Atom
- Silicon Interstitial
- Vacancy or Schottky Defect
- Impurity in Interstitial Site
- Frenkel Defect
Dislocation Defects
From Sand to Wafer

- Quartz sand: silicon dioxide
- Sand to metallic grade silicon (MGS)
- React MGS powder with HCl to form TCS
- Purify TCS by vaporization and condensation
- React TCS to $H_2$ to form polysilicon (EGS)
- Melt EGS and pull single crystal ingot
From Sand to Wafer (cont.)

• Cut end, polish side, and make notch or flat
• Saw ingot into wafers
• Edge rounding, lap, wet etch, and CMP
• Laser scribe

• Epitaxy deposition
From Sand to Silicon

Heat (2000°C)

\[ \text{SiO}_2 + \text{C} \rightarrow \text{Si} + \text{CO}_2 \]

Sand + Carbon = MGS + Carbon Dioxide
Silicon Purification I

\[ \text{Si} + \text{HCl} \rightarrow \text{TCS} \]

- Reactor, 300 °C
- Silicon Powder
- Pure TCS with 99.9999999%
Polysilicon Deposition, EGS

Heat (1100°C)

\[
\text{SiHCl}_3 + \text{H}_2 \rightarrow \text{Si} + 3\text{HCl}
\]

TCS    Hydrogen    EGS    Hydrochloride
Silicon Purification II

\[ \text{TCS} + H_2 \rightarrow \text{EGS} + \text{HCl} \]

- Process Chamber
- EGS
- Carrier gas bubbles
- Liquid TCS
- \( H_2 \) and TCS
- \( H_2 \)
Electronic Grade Silicon

Source: http://www.fullman.com/semiconductors/_polysilicon.html
Crystal Pulling: CZ method

Quartz Crucible

Graphite Crucible

Single Crystal Silicon Seed

Single Crystal silicon Ingot

Molten Silicon
1415 °C

Heating Coils
CZ Crystal Pullers

Mitsubish Materials Silicon

Source: http://www.fullman.com/semiconductors/_crystalgrowing.html
CZ Crystal Pulling

Source: http://www.fullman.com/semiconductors/_crystalgrowing.html

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Floating Zone Method

- Poly Si Rod
- Molten Silicon
- Single Crystal Silicon
- Seed Crystal
- Heating Coils Movement
- Heating Coils
Comparison of the Two Methods

• CZ method is more popular
  – Cheaper
  – Larger wafer size (300 mm in production)
  – Reusable materials

• Floating Zone
  – Pure silicon crystal (no crucible)
  – More expensive, smaller wafer size (150 mm)
  – Mainly for power devices.
Ingot Polishing, Flat, or Notch

Flat, 150 mm and smaller

Notch, 200 mm and larger
Wafer Sawing

- Orientation
- Notch
- Saw Blade
- Coolant
- Crystal Ingot
- Ingot Movement
- Diamond Coating
# Parameters of Silicon Wafer

<table>
<thead>
<tr>
<th>Wafer Size (mm)</th>
<th>Thickness (μm)</th>
<th>Area (cm²)</th>
<th>Weight (grams)</th>
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</thead>
<tbody>
<tr>
<td>50.8 (2 in)</td>
<td>279</td>
<td>20.26</td>
<td>1.32</td>
</tr>
<tr>
<td>76.2 (3in)</td>
<td>381</td>
<td>45.61</td>
<td>4.05</td>
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<tr>
<td>100</td>
<td>525</td>
<td>78.65</td>
<td>9.67</td>
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<tr>
<td>125</td>
<td>625</td>
<td>112.72</td>
<td>17.87</td>
</tr>
<tr>
<td>150</td>
<td>675</td>
<td>176.72</td>
<td>27.82</td>
</tr>
<tr>
<td>200</td>
<td>725</td>
<td>314.16</td>
<td>52.98</td>
</tr>
<tr>
<td>300</td>
<td>775</td>
<td>706.21</td>
<td>127.62</td>
</tr>
</tbody>
</table>
Wafer Edge Rounding

Wafer Before Edge Rounding

Wafer After Edge Rounding
Wafer Lapping

- Rough polished
- conventional, abrasive, slurry-lapping
- To remove majority of surface damage
- To create a flat surface
Wet Etch

- Remove defects from wafer surface
- 4:1:3 mixture of HNO₃ (79 wt% in H₂O), HF (49 wt% in H₂O), and pure CH₃COOH.
- Chemical reaction:

\[
3 \text{ Si} + 4 \text{ HNO}_3 + 6 \text{ HF} \rightarrow 3 \text{ H}_2\text{SiF}_6 + 4 \text{ NO} + 8 \text{ H}_2\text{O}
\]
Chemical Mechanical Polishing

- Pressure
- Wafer Holder
- Wafer
- Polishing Pad
- Slurry
200 mm Wafer Thickness and Surface Roughness Changes

- After Wafer Sawing
  - 76 μm
  - 914 μm

- After Edge Rounding
  - 76 μm
  - 914 μm

- After Lapping
  - 12.5 μm
  - 814 μm

- After Etch
  - <2.5 μm
  - 750 μm

- After CMP
  - Virtually Defect Free
  - 725 μm

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Epitaxy Grow

• Definition
• Purposes
• Epitaxy Reactors
• Epitaxy Process
Epitaxy: Definition

- Greek origin
- *epi*: upon
- *taxy*: orderly, arranged

- Epitaxial layer is a single crystal layer on a single crystal substrate.
Epitaxy: Purpose

• Barrier layer for bipolar transistor
  – Reduce collector resistance while keep high breakdown voltage.
  – Only available with epitaxy layer.

• Improve device performance for CMOS and DRAM because much lower oxygen, carbon concentration than the wafer crystal.
Epitaxy Application, Bipolar Transistor

Electron flow
n⁺ Buried Layer

SiO₂
p⁺
n⁺
p
n⁺
p⁺

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Epitaxy Application: CMOS

P-Wafer

N-Well

P-Well

P-type Epitaxy Silicon

Metal 1, Al•Cu

BPSG

W

n^+

n^+

p^+

p^+
Silicon Source Gases

Silane
Dichlorosilane
Trichlorosilane
Tetrachlorosilane

$\text{SiH}_4$
$\text{SiH}_2\text{Cl}_2$
$\text{SiHCl}_3$
$\text{SiCl}_4$
Dopant Source Gases

Diborane        \( \text{B}_2\text{H}_6 \)
Phosphine       \( \text{PH}_3 \)
Arsine          \( \text{AsH}_3 \)
DCS Epitaxy Grow, Arsenic Doping

Heat (1100 °C)

\[ \text{SiH}_2\text{Cl}_2 \rightarrow \text{Si} + 2\text{HCl} \]

DCS  Epi  Hydrochloride

Heat (1100 °C)

\[ \text{AsH}_3 \rightarrow \text{As} + 3/2 \text{H}_2 \]
Schematic of DCS Epi Grow and Arsenic Doping Process
Epitaxial Silicon Growth Rate Trends

Temperature (°C)

Growth Rate, micron/min

0.7 0.8 0.9 1.0 1.1

SiH₂Cl₂

SiHCl₃

SiH₄

Mass transport limited

Surface reaction limited

1000/T(K)
Barrel Reactor

Radiation
Heating Coils

Wafers
Vertical Reactor

Heating Coils

Reactants

Wafers

Reactants and byproducts
Horizontal Reactor

Reactants

Heating Coils

Wafers

Reactants and byproducts
Epitaxy Process, Batch System

- Hydrogen purge, temperature ramp up
- HCl clean
- Epitaxial layer grow
- Hydrogen purge, temperature cool down
- Nitrogen purge
- Open Chamber, wafer unloading, reloading
Single Wafer Reactor

• Sealed chamber, hydrogen ambient
• Capable for multiple chambers on a mainframe
• Large wafer size (to 300 mm)
• Better uniformity control
Single Wafer Reactor

Heat Radiation

Heating Lamps

Reactants

Susceptor

Quartz Window

Reactants & byproducts

Quartz Lift Fingers

Waffer
Epitaxy Process, Single Wafer System

- Hydrogen purge, clean, temperature ramp up
- Epitaxial layer grow
- Hydrogen purge, heating power off
- Wafer unloading, reloading

- In-situ HCl clean,
Why Hydrogen Purge

- Most systems use nitrogen as purge gas
- Nitrogen is a very stable abundant
- At > 1000 °C, N₂ can react with silicon
- SiN on wafer surface affects epi deposition
- H₂ is used for epitaxy chamber purge
- Clean wafer surface by hydrides formation
## Properties of Hydrogen

<table>
<thead>
<tr>
<th>Name</th>
<th>Hydrogen</th>
</tr>
</thead>
<tbody>
<tr>
<td>Symbol</td>
<td>H</td>
</tr>
<tr>
<td>Atomic number</td>
<td>1</td>
</tr>
<tr>
<td>Atomic weight</td>
<td>1.00794</td>
</tr>
<tr>
<td>Discoverer</td>
<td>Henry Cavendish</td>
</tr>
<tr>
<td>Discovered at</td>
<td>England</td>
</tr>
<tr>
<td>Discovery date</td>
<td>1766</td>
</tr>
<tr>
<td>Origin of name</td>
<td>From the Greek words &quot;hydro&quot; and &quot;genes&quot; meaning &quot;water&quot; and &quot;generator&quot;</td>
</tr>
<tr>
<td>Molar volume</td>
<td>11.42 cm³</td>
</tr>
<tr>
<td>Velocity of sound</td>
<td>1270 m/sec</td>
</tr>
<tr>
<td>Refractive index</td>
<td>1.000132</td>
</tr>
<tr>
<td>Melting point</td>
<td>-258.99°C</td>
</tr>
<tr>
<td>Boiling point</td>
<td>-252.72°C</td>
</tr>
<tr>
<td>Thermal conductivity</td>
<td>0.1805 W m⁻¹ K⁻¹</td>
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</table>

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Defects in Epitaxy Layer

Stacking Fault from Surface Nucleation

Dislocation

Impurity Particle

Hillock

Stacking Fault form Substrate Stacking Fault

Epi Layer

Substrate

After S.M. Zse’s *VLSI Technology*

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Future Trends

- Larger wafer size
- Single wafer epitaxial grow
- Low temperature epitaxy
- Ultra high vacuum (UHV, to $10^{-9}$ Torr)
- Selective epitaxy
Summary

• Silicon is abundant, cheap and has strong, stable and easy grown oxide.
• \(<100>\) and \(<111>\)
• CZ and floating zone, CZ is more popular
• Sawing, edging, lapping, etching and CMP
Summary

• Epitaxy: single crystal on single crystal
• Needed for bipolar and high performance CMOS, DRAM.
• Silane, DCS, TCS as silicon precursors
• $\text{B}_2\text{H}_6$ as P-type dopant
• $\text{PH}_3$ and $\text{AsH}_3$ as N-type dopants
• Batch and single wafer systems