Chapter 2

Introduction of IC Fabrication

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Objectives

- Define yield and explain its importance
- Describe the basic structure of a cleanroom.
- Explain the importance of cleanroom protocols
- List four basic operations of IC processing
- Name at least six process bays in an IC fab
- Explain the purposes of chip packaging
- Describe the standard wire bonding and flip-chip bump bonding processes
Wafer Process Flow

- Materials
- Wafers
- Masks
- Design
- IC Fab
- Metallization
- CMP
- Dielectric deposition
- Thermal Processes
- Implant PR strip
- Etch PR strip
- Photo-lithography
- Test
- Packaging
- Final Test
Fab Cost

• Fab cost is very high, > $1B for 8” fab
• Clean room
• Equipment, usually > $1M per tool
• Materials, high purity, ultra high purity
• Facilities
• People, training and pay
Wafer Yield

\[ Y_W = \frac{Wafers_{\text{good}}}{Wafers_{\text{total}}} \]
Die Yield

\[ Y_D = \frac{Dies_{\text{good}}}{Dies_{\text{total}}} \]
Packaging Yield

\[ Y_C = \frac{Chips_{\text{good}}}{Chips_{\text{total}}} \]
Overall Yield

\[ Y_T = Y_W \times Y_D \times Y_C \]

Overall Yield determines whether a fab is making profit or losing money
How Does Fab Make (Loss) Money

• Cost:
  – Wafer (8”): ~$150/wafer*
  – Processing: ~$1200 ($2/wafer/step, 600 steps)
  – Packing: ~$5/chip

• Sale:
  – ~200 chips/wafer
  – ~$50/chip (low-end microprocessor in 2000)

*Cost of wafer, chips per wafer, and price of chip varies, numbers here are choosing randomly based on general information.
## How Does a Fab Make *(Loss)* Money

<table>
<thead>
<tr>
<th></th>
<th>100% yield: 150+1200+1000 = $2350/wafer</th>
<th>50% yield: 150+1200+500 = $1850/wafer</th>
<th>0% yield: 150+1200 = $1350/wafer</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Cost:</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Sale:</strong></td>
<td>100% yield: 200×50 = $10,000/wafer</td>
<td>50% yield: 100×50 = $5,000/wafer</td>
<td>0% yield: 0×50 = $0.00/wafer</td>
</tr>
<tr>
<td><strong>Profit Margin:</strong></td>
<td>10000 − 2350 = $7650/wafer</td>
<td>5000 − 1850 = $3150/wafer</td>
<td>0 − 1350 = −$1350/wafer</td>
</tr>
</tbody>
</table>
Question

• If yield for every process step is 99%, what is the overall processing yield after 600 process steps?
Answer

• It equals to 99% times 99% 600 times

• \(0.99^{600} = 0.0024 = 0.24\%\)

• Almost no yield
Throughput

• Number of wafers able to process
  – Fab: wafers/month (typically 10,000)
  – Tool: wafers/hour (typically 60)
• At high yield, high throughput brought
Defects and Yield

\[ Y \propto \frac{1}{(1 + DA)^n} \]
Yield and Die Size

Killer Defects

\[ Y = \frac{28}{32} = 87.5\% \quad Y = \frac{2}{6} = 33.3\% \]
Illustration of a Production Wafer

Die

Test die
Illustration of a Production Wafer

Test Structures

Scribe Lines

Dies
Clean Room

• Artificial environment with low particle counts
• Started in medical application for post-surgery infection prevention

• Particles kills yield
• IC fabrication must in a clean room
Clean Room

• First used for surgery room to avoid bacteria contamination

• Adopted in semiconductor industry in 1950

• Smaller device needs higher grade clean room

• Less particle, more expensive to build
Clean Room Class

- Class 10 is defined as less than 10 particles with diameter larger than 0.5 μm per cubic foot.
- Class 1 is defined as less than 1 such particles per cubic foot.
- 0.18 mm device require higher than Class 1 grade clean room.
Cleanroom Classes

# of particles / ft³

Particle size in micron

Class M-1

Class 1

Class 10

Class 100

Class 1,000

Class 10,000

Class 100,000

Class 100,000

Class 10,000

Class 1,000

Class 100

Class 10

Class 1

Class M-1
# Definition of Airborne Particulate Cleanliness Class per Fed. Std. 209E

<table>
<thead>
<tr>
<th>Class</th>
<th>Particles/ft$^3$</th>
<th>0.1 μm</th>
<th>0.2 μm</th>
<th>0.3 μm</th>
<th>0.5 μm</th>
<th>5 μm</th>
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</thead>
<tbody>
<tr>
<td>M-1</td>
<td></td>
<td>9.8</td>
<td>2.12</td>
<td>0.865</td>
<td>0.28</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
<td>35</td>
<td>7.5</td>
<td>3</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td></td>
<td>350</td>
<td>75</td>
<td>30</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>100</td>
<td></td>
<td>750</td>
<td>300</td>
<td>100</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1000</td>
<td></td>
<td></td>
<td></td>
<td>1000</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td>10000</td>
<td></td>
<td></td>
<td></td>
<td>10000</td>
<td>70</td>
<td></td>
</tr>
</tbody>
</table>
Effect of Particles on Masks

Particles on Mask

Stump on +PR

Hole on −PR

Film

Substrate

Film

Substrate
Effect of Particle Contamination

- Ion Beam
- Dopant in PR
- Photoresist
- Screen Oxide
- Partially Implanted Junctions
- Particle
Cleanroom Structure

- Makeup Air
- Fans
- Equipment Area Class 1000
- Process Tool
- HEPA Filter
- Process Area Class 1
- Equipment Area Class 1000
- Raised Floor with Grid Panels
- Pump, RF and etc.
- Return Air
Mini-environment

- Class 1000 cleanroom, lower cost
- Boardroom arrangement, no walls between process and equipment
- Better than class 1 environment around wafers and the process tools
- Automatic wafer transfer between process tools
Mini-Environment Cleanroom

Makeup Air

HEPA Filter

Class 1000

Process Tool

HEPA Filter

Class 1

Process Tool

Raised Floor with Grid Panels

Return Air

Fans

Pump, RF and etc.

Makeup Air
Gowning Area

- Shelf of Gloves, Hair and Shoe Covers
- Gown Racks
- Disposal Bins
- Entrance
- Wash/Clean Stations
- Storage
- Benches
- To Cleanroom
- Shelf of Gloves
- Shelf of Gloves
IC Fabrication Process Module

- Thin film growth, dep. and/or CMP
- Photolithography
  - Etching
  - PR Stripping
  - Ion Implantation
  - PR Stripping
  - RTA or Diffusion
Illustration of Fab Floor

- Equipment Areas
- Process Bays
- Corridor
- Sliding Doors
- Gowning Area
- Service Area
Mini-environment Fab Floor
Wet Processes

Etch, PR strip, or clean

Rinse

Dry
Horizontal Furnace

Quartz Tube

Heating Coils

Wafers

Center Zone

Flat Zone

Temperature

Distance

Gas flow
Vertical Furnace

- Process Chamber
- Heaters
- Wafers
- Tower
Schematic of a Track Stepper Integrated System

- Prep Chamber
- Spin Coater
- Chill Plates
- Stepper
- Hot Plates
- Wafer Movement
- Wafer
- Chill Plates
Cluster Tool with Etch and Strip Chambers

PR Strip Chamber

Etch Chamber

Robot

Transfer Chamber

Loading Station

Unloading Station
Cluster Tool with Dielectric CVD and Etchback Chambers

O$_3$-TOES Chamber

Ar Sputtering Chamber

PECVD Chamber

Robot

Transfer Chamber

Loading Station

Unloading Station
Cluster Tool with PVD Chambers

Al·Cu Chamber

Ti/TiN Chamber

Robot

Transfer Chamber

Loading Station  Unloading Station
Dry-in Dry-out CMP System

- Wafer Loading and Standby
- Post-CMP Clean
- Rinse
- Dryer and Wafer Unloading
- Clean Station
- Multi-head Polisher
- Polishing Pad
- Polishing Heads

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Process Bay and Equipment Areas

- Sliding Doors
- Process Tools
- Tables For PC and Metrology Tools
- Service Area
- Wafer Loading Doors
Test Results

Failed die
Chip-Bond Structure

Microelectronics Devices and Circuits

Chip Backside Metallization

Chip (Silicon)

Solder

Substrate (Metal or Ceramic)

Substrate Metallization

Melt and Condense
Wire Bonding

- Metal Wire
- Formation of molten metal ball
- Bonding Pad
- Wire Clamp
- Press to make contact
- Bonding Pad
- Head retreat

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Wire Bonding

Lead contact with pressure and heat

Clamp closed with heat on to break the wire
IC Chip with Bonding Pads

Bonding Pads
IC Chip Packaging

Chip
Bonding
Pad
Pins
Chip with Bumps
Flip Chip Packaging

Bumps

Chip

Socket

Pins
Bump Contact
Heating and Bumps Melt

Diagram showing bumps between a chip and socket pins.
Flip Chip Packaging

Chip

Socket   Pins
Molding Cavity for Plastic Packaging

Top Chase

Molding Cavity

Bonding Wires

IC Chip

Lead Frame

Chip Bond Metallization

Bottom Chase
Ceramic Seal

- Bonding Wires
- IC Chip
- Cap Seal Metallization
- Layer 2
- Lead Frame, Layer 1
- Pins
- Chip Bond Metallization
Summary

• Overall yield
• Yield determines losing money or making profit
• Cleanroom and cleanroom protocols
• Process bays
• Process, equipment, and facility areas
• Die test, wafer thinning, die separation, chip packaging, and final test