Comprehensive Low-Frequency and RF Noise Characteristics in Strained-Si NMOSFETs


Abstract

Due to the mobility enhancement of strained-Si channel, the strained-Si MOSFET has reportedly a great improvement on DC characteristics. The improvement on the cut-off frequency ($f_T$) of strained-Si device is demonstrated in this work. The strained-Si device has the same flicker noise ($1/f$) as the control Si device as long as no threading dislocation exists in the channel and the thermal budget is properly controlled. The large density of defect in the relaxed SiGe buffer layers shows no effect on the flicker noise. The threading dislocation penetrating into the strained-Si channel and Ge outdiffusion can degrade the flicker noise of strained-Si NMOSFETs. A thicker strained-Si channel layer can reduce the roughness scattering from the underneath strained Si/relaxed SiGe heterojunction, and yields a higher mobility, higher $f_T$, and lower noise figures, as compared to the thin strained-Si channel.

Introduction

With the fast growth in the wireless communication market, RF devices with high performance but low cost are highly demanded. Recently, strained-Si MOSFETs with high performance on DC characteristics have been reported [1]. The mobility enhancement of strained-Si can be as high as 110% at the electrical field of 1.4 MV/cm [2]. However, the corresponding enhancement on $f_T$ is as critical to obtain the superior RF performance. The large current drive of strained-Si device improves amplification performance, and the high $f_T$ increases the application bandwidth. Noise figure is crucial for low noise amplifier, and $1/f$ noise is a key factor to determine the phase noise of voltage control oscillator. Therefore, different device sizes, channel structures, and process flows are used to study $f_T$, the $1/f$ noise, and noise figure. As a result, the device without threading dislocation in the channel shows no degradation on $1/f$ noise. For sub-100nm devices, even with the dislocation density of $1 \times 10^6$ cm$^{-2}$, the threading dislocation are hardly found in the channel, and therefore, the $1/f$ noise performance is not degraded. However, to ensure the circuit performance and yield, the position of threading dislocation should be controlled to avoid the penetration to $1/f$ noise-sensitive circuit areas. The thicker strained-Si channel can yield higher $f_T$, lower noise figure, and higher $G_m$ due to the weaker interface roughness scattering at strained Si/relaxed SiGe heterojunction. Therefore, the flattening of relaxed SiGe buffer layers by CMP seems not crucial if the oxide/strained Si interface roughness can be minimized and the strained-Si channel is thick enough.

Material and Devices Characteristics

The 12-24 nm strained-Si channel is grown on relaxed Si$_{0.8}$Ge$_{0.2}$ buffer layers by UHV/CVD and the strain in Si is measured by surface Raman spectroscopy (Fig. 1), indicating a strain of ~0.64%. The tensile strain increases to 0.7% after the device process thermal budget due to the additional relaxation of SiGe buffer layers. The 30nm LTO (TEOS, 700°C) was used as the gate oxide to avoid high temperature process. For comparison, 5 nm RTO oxide (900°C, 5 min) is also used. The output characteristics of the strained-Si shows a ~78% and ~35% increase of $I_{DS}$ in the linear and the saturation region, respectively, at constant overdrive. The threshold voltage of strained-Si shows negative ~0.14 V shift with respect to control Si, corresponding to a conduction band offset of ~0.12 V at strained-Si/relaxed SiGe heterojunction for Ge content 20% [3]. The electron effective mass was extracted from drain current and split-CV measurements on a large-area device, and shows a 65% enhancement at 1.0 MV/cm as shown in Fig. 2.

Low-Frequency Noise

Fig. 3 shows the drain current noise ($S_{ID}$) of both strained-Si and control Si devices. The $S_{ID}$ increases with the gate width due to the adjacent unit current density correlation [4]. The threading defect density is ~1x10$^6$ cm$^{-2}$ observed by defect etching measurement. This indicates that the average distance of the threading dislocation penetrating into the strained-Si channel is about 10 µm. The main source of low-frequency flicker noise is the capture and release of carriers in the traps. For small area devices (WxL ≤ 100 µm$^2$), where there is almost no threading dislocation in the channel, the strained-Si device has a similar flicker noise of the $S_{ID}$ to that of the control device (inset of Fig. 3). For large devices (WxL= 25x25 µm$^2$), there are possibly threading dislocations in the channel, and the strained-Si device has a larger flicker noise (10x) than the control device (inset of Fig. 4). Both strained-Si and control devices exhibit similar $S_{ID}$ for these small area devices (L=0.6, 0.8, 1.2 µm). In Fig. 4, the $S_{ID}$ for strained-Si and control devices decreases as the gate length increases due to velocity saturation and hot electron effects.
In Fig. 5, the strained-Si device with a large area has a larger flicker noise as compared to the control device, since it is more susceptible to the penetration of threading dislocation into its channel. A small area strained-Si device without threading dislocation in the channel has the same flicker noise as the control device. Significant flicker noise increase of the strained-Si device as compared to control device is found for the device area larger than 100 µm² as shown in Fig. 6. This clearly shows that the threading dislocations in the channel are responsible for the flicker noise increase.

The small area strained-Si device with RTO as gate dielectrics exhibits a much larger flicker noise than the control device (Fig. 7). The high temperature RTO process will inject the Si interstitials into the underneath Si/SiGe heterojunction, and enhances the Ge outdiffusion into the Si/oxide interface to form trap centers [5]. In Fig. 8, the strained-Si device with TEOS has a clear hole confinement shoulder in the accumulation region of the quasi-static C-V curves at various temperatures, indicating good abruptness of the Si/SiGe heterojunction. For the strained-Si device with RTO, no such hole confinement shoulder is observed (inset of Fig. 8), indicating that the Si/SiGe heterojunction in the RTO devices is smeared out due to Ge outdiffusion at high temperature. The $D_n$ of both strained-Si and control Si devices with TEOS and RTO oxide are extracted from high-low frequency C-V method (Fig. 9). For control Si devices, the RTO device has a lower $D_n$ as compared to the TEOS device due to the high temperature process. However, the strained-Si device with RTO has a much higher $D_n$ than the control device with RTO, while for TEOS devices, both the strained-Si device and the control device have similar $D_n$. Such contrast implies that the trap is formed due to the Ge outdiffusion into SiO₂/strained-Si interface. Besides, no thickness dependence of strained Si on $S_{md}$ is observed for the strained-Si device. This suggests again that the source of the flicker noise is the threading dislocation. The $S_{md}$ of strained-Si with a doping concentration of $1 \times 10^{17}$ cm⁻³ reveals a slightly higher flicker noise (~1.5x) than that of $1 \times 10^{16}$ cm⁻³, indicating a small effect of the dopant impurities in the channel.

RF Noise

The flicker noise mainly affects the performance of the device at low frequency and can be ignored at high frequency. When working at high frequency, the thermal noise generated within the device itself will play an important role in the overall system characteristics, especially for front-end receivers. The minimum noise figures (NF min) of the strained-Si and the control Si device are shown in Fig. 10. For measurement data without de-embedding (Fig. 10), the strained-Si device has an improved noise figure at low field (<50 kV/cm), but has a larger noise figure than the control device at high field (>50 kV/cm). Note that the strained-Si device has a higher $G_m$ (~35 % at peak) and $f_t$ (~12 % at peak) than the control device (inset of Fig. 10). The cause of this behavior is still unknown. Possible origins include different doping level ($1 \times 10^{16}$ cm⁻³ for strained-Si and $1 \times 10^{15}$ cm⁻³ for control Si), defect density, and parasitic effect. In Fig. 10, only the parasitic effect of the pad is de-embedded from the measurement data, and the other parameters, e.g. $R_g$, $R_s$, $R_D$, $C_{GB}$, $C_{DB}$, $C_{SB}$, etc, still exist. Therefore, the de-embedded data are not equivalent to intrinsic channel noise. Note that the data are collected at the saturation region, which is different from the mobility extraction in linear region (Fig. 2).

The increase of strained-Si thickness can improve the NF min as shown in Fig. 11, since a thick strained-Si implies that the electron channel is far away from the Si/SiGe heterojunction, and thus has a higher mobility (Fig. 12), higher $G_m$, and higher $f_t$ (inset of Fig.11). The interface roughness (~7 nm) of Si/SiGe heterostructure scatters the electrons if the electrons are too close to the heterojunction. After the strained-Si channel layer is deposited, the as-grown surface roughness decreases to 4.5-5.5 nm for different strained-Si thickness devices. Since the final roughness (~5.5 nm) of strained-Si surface after the device processing is similar for different strained-Si thickness (12-24 nm), the electron scattering by the roughness at Si/oxide interface should also be similar for different strained-Si thickness devices. The increase of the surface roughness after the device thermal budget is due to the additional relaxation of SiGe buffer layers, which yields a larger strain in strained Si after thermal process, as confirmed by Raman spectroscopy. All the strained-Si devices with different strained-Si thickness using TEOS as gate oxides have shoulders in the quasi-static C-V curves, indicating good abruptness of the Si/SiGe heterojunction.

Summary

The enhanced DC characteristics and improved $f_t$ performance of strained-Si as compared with control Si NMOSFETs have been demonstrated. The threading dislocation penetrating into the strained-Si channel and Ge outdiffusion from the Si/SiGe heterojunction to the Si/oxide interface can increase the flicker noise of strained-Si devices. The NF min can be further improved with increasing strained-Si layer thickness. The higher mobility (~65 % enhancement), higher $G_m$ (~33 %) and higher $f_t$ (~12 %) of strained-Si devices, make it possible to have better CMOS RF performance than SiGe/Si BiCMOS.

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References

Fig. 1. Raman spectrum of the strained-Si on relaxed Si$_{0.8}$Ge$_{0.2}$ buffer layer. The position of Si-Si peak of strained-Si indicates a 0.64% tensile strain.

Fig. 2. Effective mobility of strained-Si, which is enhanced by 65% over control Si at the effective electrical field of 1.0MV/cm.

Fig. 3. The spectral density of drain current noise for the strained-Si and the control devices with different gate widths (W). Device area ≤ 20µm$^2$.

Fig. 4. The spectral density of drain current noise for the strained-Si and the control devices with different gate lengths (L).

Fig. 5. (a) A large area device with threading dislocation in the channel. (b) A small area device without threading dislocation.

Fig. 6. The $S_{ID}$ ratio of the strained-Si to the Si control vs device area.
Fig. 7. The $S_{ID}$ of the strained-Si and the control devices with 5nm, 900°C RTO as gate dielectrics. The strained-Si device has a higher $S_{ID}$ than the control device.

Fig. 8. Quasi-static C-V measurement of strained Si devices. The hole confinement is clearly observed in the C-V curves of TEOS devices but is not in RTO device due to Ge outdiffusion.

Fig. 9. The $D_{it}$ increases due to Ge outdiffusion. The strained-Si with RTO has a highest $D_{it}$ of $8 \times 10^{11}$ eV$^{-1}$ cm$^{-2}$ due to the oxidation-enhanced Ge outdiffusion.

Fig. 10. The $NF_{min}$ vs. vertical E-field of strained-Si and control Si. The table of the inset lists the peak $G_m$ and $f_t$. Note that the channel dopings for strained-Si and control Si are $1 \times 10^{16}$ cm$^{-3}$ and $1 \times 10^{15}$ cm$^{-3}$, respectively.

Fig. 11. The $NF_{min}$ vs. vertical E-field of strained-Si for thickness=12nm, 18nm, and 24nm. The peak $G_m$ and $f_t$ are listed in the table of the inset. The channel doping is $1 \times 10^{15}$ cm$^{-3}$.

Fig. 12. The mobility of strained-Si device with thickness of 12, 18, and 24nm. The electron in the thinner strained-Si channel suffers more roughness scattering from Si/SiGe heterojunction.