Atomic-scale planarization of \( \text{SiO}_2/\text{Si}(001) \) interfaces

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In ultralarge-scale integrated circuit (ULSI) technology, planarization of silicon surfaces has recently been extensively studied. This is because the surfaces strongly depend on the precleaning procedure. The gate oxide thickness has become smaller and substrate doping levels have become larger owing to the decreased size of ULSIs. Also two-dimensional channel electrons within shallower inversion layers may easily be scattered by the \( \text{Si}/\text{SiO}_2 \) interface roughness. As can be seen in several works, this causes the degradation of the channel mobility even at room temperature. However, in contrast to a relatively thick oxide, the \( \text{SiO}_2 \) growth mechanism is not so well known as for the thin oxide regime (\(< 10 \) nm) where a different model is thought to be required. In this letter, we report on the extremely thin oxide formation with atomically flat \( \text{Si}/\text{SiO}_2 \) interfaces.

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P-type \([ \text{B doped, } 9 \ \Omega \ \text{cm}] \) (001) Si wafers were used and two types of preparation were employed in this experiment, i.e., standard "wet cleaned" and "UHV (ultrahigh vacuum) cleaned" samples. The wet clean samples were produced by the conventional RCA cleaning method and subsequent thermal oxidation in a dry oxygen ambient at 900 °C for various oxidation time. The \( \text{SiO}_2 \) thickness (\( T_{\text{ox}} \)) is examined up to 50 nm. As for the "UHV clean" samples, the substrate was cut into rectangular shapes (\( 4 \times 12 \) mm\(^2 \)) after the RCA clean. These pieces were then introduced into the UHV environment (\( 4 \times 10^{-11} \) Torr) through a loadlock chamber. After degassing, by resistive heating, the samples were flash heated at 1200 °C for a few seconds in order to obtain the reconstructed \( 2 \times 1 \) surface. After cooling to room temperature in UHV, they were removed and kept in a dust-free space in air. Finally, these samples were also oxidized in a same condition as wet clean samples. The reconstructed surface was observed by scanning tunneling microscopy in an ultrahigh vacuum (UHV-STM; OMCIRON Vacuum Physik GMBH) in order to confirm the surface morphology. For the UHV-STM, an electrochemically polished W tip was used. And a bias was applied to the sample surface with the tunneling current of 0.5 nA. For both types of samples, observation of the silicon-oxide interface was performed by means of cross-sectional transmission electron microscope (XTEM; ABT-EM-002B) with an accelerating voltage of 200 kV and a resolution of 0.19 nm. After the oxidation, XTEM samples were prepared by depositing a polysilicon cap layer by means of chemical vapor deposition (CVD) at 600 °C for 30 min and thinning the sample by means of Ar ion milling to less than 15 nm. The observation was performed by high-resolution lattice imaging in the [100] Si substrate orientation. No image degradation with time was found for the present conditions.

From the XTEM micrograph for the silicon-oxide interface, the position of the interface boundary (center of the topmost Si lattice image spot) was digitized. The fluctuation sequence of the roughness is determined by a distance from a least-square line of the boundary to the respective position of the interface boundary. The least square line was calculated from the distance between an arbitrary [110] line and the interface boundary. For the sequence, the autocovariance function (ACF) can be estimated in order to quantify the interface roughness parameter, i.e., rms roughness (\( \Delta \)) and correlation length (\( L \)). In this letter, we mainly refer to the former. We will discuss the latter elsewhere. A zeroth coefficient of the ACF is the square of the root mean square fluctuation of the interface roughness \( \Delta \).

Figure 1 shows the XTEM micrograph. The rms roughness (\( \Delta \)) of the original surface prior to the RCA cleaning with a 0.7 nm thick native oxide [Fig. 1(a)] was 0.16 nm which might be determined by the final polishing process. (b) of this figure shows one example of a wet clean sample with a dry oxide thickness (\( T_{\text{ox}} \)) of 4.29 nm. The rms fluctuation of the silicon-oxide interface (\( \Delta \)) was 0.26 nm. At the initial stage of the oxidation, the interface of the wet clean samples appeared to be a steplike undulation superimposed on a large wavelength undulation becoming a more undulating boundary when \( T_{\text{ox}} \) is increased. In contrast, as shown in Fig. 1(c), the UHV clean sample...
showed atomically flat interface with $A=0.1$ nm for $T_{\text{ox}}=4.61$ nm, indicating step-by-step fluctuation determined by the off-angle of the substrate.

Figure 2(a) shows a UHV-STM image for Si(001)-2×1 reconstructed clean surface prepared by flashing in UHV. The surface consists of the top-most silicon dimer rows forming atomically flat terraces where the dimer rows run parallel and perpendicular to the picture diagonal on alternate terraces. The terrace is separated by monoatomic steps (0.136 nm) and the interval along [100] is in the range 10–30 nm indicating that off angle ($\theta$) is $\sim0.26$–0.78$^\circ$. The surface defect density seems to depend on the heating procedure in UHV, and as shown in (b) of this figure. Atomic force microscopy (AFM) was introduced in order to study the surface morphology after the native oxide growth on moving the reconstructed surface into air. There are faint vestiges of steplike features which are also separated by about 30 nm, consistent with the image of the 2×1 reconstructed surface in Fig. 2(a). As far as the step configuration is concerned, this implies that the underlying reconstructed Si surface morphology is unchanged after the native oxide growth. This is consistent with results of the other AFM experiments.\textsuperscript{15}

The oxide thickness dependency of the roughness for these two types of samples was investigated as demonstrated in Fig. 3. In the case of wet clean samples, the interfaces tend to become rough up to a maximum value at around $T_{\text{ox}}=4$ nm and smooth after this thickness. Further interface roughening was not observed for the thicker oxide range. When $T_{\text{ox}}=50$ nm, $A=0.16$ nm for wet clean samples. This is considered to be due to the balance between parameters increasing the roughness (such as initial surface irregularities, local fluctuations in the interface reaction rate, and the lack of stress relief during oxidation) and parameters reducing it (such as transition to diffusion limited processes for thicker oxides, stress relaxation at high temperatures, and a less localized strain distribution). Similar results were suggested by the work of Carim and Sinclair in a similar oxidation regime.

Whereas, the UHV clean samples revealed atomically flat interfaces over the observed thickness range ($T_{\text{ox}}<10$ nm), the interface roughness ($A$) increases gradually with increasing $T_{\text{ox}}$. XTEM micrographs of the samples when $T_{\text{ox}}=1.00$ nm show there were no atomic steps over 50 nm in the [110] direction. The rms roughness ($\Delta$) was 0.072

![FIG. 1. XTEM image of a (a) bare Si(001) after the RCA cleaning with native oxide, (b) dry SiO$_2$ (4.29 nm)-Si interface of a wet clean sample, and (c) dry SiO$_2$ (4.61 nm)-Si interface of a UHV clean sample.](image1)

![FIG. 2. UHV-STM image of a Si(001)-2×1 reconstructed clean surface.](image2)

![FIG. 3. Oxide thickness dependence for the interface roughness ($A$).](image3)
nm. Similarly, when \( T_{\text{ox}} = 3.43 \) nm, the interface still appears atomically flat (\( \Delta = 0.094 \) nm) in comparison with the wet clean samples. For further oxidation, gradual increases of \( \Delta \) were observed. When \( T_{\text{ox}} \) approaches about 10 nm, the interface roughness (\( \Delta \)) for both types of sample tends to approach \( \sim 0.16 \) nm and seems to saturate at this value. As for the ACF characteristics, the decay behavior indicated “exponential” throughout this oxide thickness range for the UHV clean samples. We will discuss it in detail elsewhere. In this oxide thickness, the oxidation may proceed in the same way as that for wet clean samples. When \( T_{\text{ox}} = 8.89 \) nm, the interface of the UHV clean sample revealed a somewhat larger roughness (\( \Delta = 0.17 \) nm) which is almost the same value as that of the wet clean sample. At this oxide thickness, the interface did not definitely approximate an exponential or Gaussian fluctuation.

In conclusion, atomically flat planarization of a silicon-oxide interface could be accomplished after obtaining a clean surface in UHV followed by native oxide growth and successive conventional thermal oxidation. When the surface is prepared by a conventional wet cleaning prior to oxidation, the interface initially tends to become rough and gradually smooths with increasing oxide thickness. In comparison with conventional interfaces, this planarization is significant under an oxide thickness of less than \( \sim 8 \) nm. This thickness range will be extremely important for future ULSIs. Regardless of the preoxidation process, in a relatively thicker oxide range (more than 10 nm), the interface fluctuation tends to be similar and saturate to \( \Delta = 0.16 \) nm, presumably limited by the normal oxidation mechanism. Further consideration of this experiment as well as the relationship between the interface roughness and the electrical characteristics will be discussed elsewhere.

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