Wafer bonding technology for optoelectronic integrated devices

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Abstract

Wafer bonding has been investigated as a key technology to integrate InP lasers on Si for optoelectronic integrated circuits. The bonding process has been optimized to allow the integration of InGaAsP/InP double-heterostructures (DHs) on Si with keeping the crystal qualities good enough to realize the lasers. As a result, room temperature continuous-wave (CW) operation of InP edge-emitting lasers has been achieved. In addition, as one of the building blocks to implement the optimal interconnections between Si LSIs, InP optical devices on Si integrated with the back-surface diffractive lenses have been demonstrated. A novel bonding process which allows an integration on structured wafers, such as Si LSI wafers, has also been proposed. The wafer bonding is thought to be a promising technique to implement optical interconnections between Si LSI chips.

1. Introduction

Optical interconnections between Si LSI chips have been attracting increasing interest as a key technology to overcome communication bottlenecks in electrical interconnections of the future high-speed LSI system and/or to realize new functional LSI processors [1–3]. Fig. 1 schematically illustrates the proposed structure of the optically interconnected LSIs. InP lasers, preferably surface emitting lasers, are integrated on LSI chips and the optical signals are emitted through the Si substrate to another LSI chip. InP-based lasers are suitable for this application because Si is transparent at the emission wavelength. In addition, diffractive optical elements (DOEs) such as diffractive lenses and beam deflectors can be integrated on the back-surface of the Si wafer. In two-dimensional integration, the LSIs with lasers are mounted on a waveguide substrate such as glass or Si and are optically interconnected using DOEs fabricated on the Si back-surface and the waveguide substrates.

In order to realize such integrated structures, usually called as optoelectronic integrated circuits (OEICs), integrations of III-V optical devices on Si has been widely studied with several different approaches, including solder bonding [4], lattice-mismatched epitaxial growth [5,6] and wafer bonding [7,9]. Solder bonding with metals such as AuSn [4] is the most straightforward method, but it is not suitable for vertical optical interconnections (Fig. 1(a)) because the metals interrupt the vertical light propagation. Lattice-mismatched epitaxial growth has been widely investigated and room-temperature CW operation of the lasers on Si has been successfully demonstrated [5,6]. However, there are some problems in this growth technique, such as high dislocation densities (>5 × 10⁶ cm⁻²) and high growth temperatures (typically
>900°C for thermal pre-cleaning of Si and >550°C for epitaxial growth). The high growth temperatures may cause a big problem in the device integration because the interconnection metals in LSIs, especially aluminum, will be degraded when the fully processed LSIs are exposed to the temperatures higher than 500°C [10,11].

Wafer bonding is another promising candidate. It is a technique to bond different wafers by contacting the flat surfaces face-to-face after appropriate surface cleaning without using any adhesives. Since the technique was first demonstrated in 1986 for Si–Si bonding [12] and the fabrication of silicon-on-insulator (SOI) structures [13], it has been extensively investigated mainly for Si-based materials, and has recently been applied to other materials including InP–GaAs [14–16], GaAs–Si [7,17], InP–Si [8,9,18,19], GaAs–LiNbO₃ [20] and LiNbO₃–LiTaO₃ [21]. With the wafer bonding technique, it is possible to bond wafers at low temperatures (even at room temperature) through Van der Waals force [7] and/or hydrogen bonding between surface OH-groups [12]. Therefore, we can integrate InP/InGaAsP materials on fully processed LSI wafers without degradation of the LSI characteristics. Additionally, optical devices can be fabricated using photolithography after wafer bonding because the bonds can be strong enough to endure following device fabrication processes. This will facilitate alignment of large number of small optical devices with Si circuits, resulting in a potentially inexpensive integrated system.

In this paper, we report on the procedures and properties of InP–Si bonding and the fabrication of InGaAsP/InP optical devices on Si. In Section 2, we review the bonding process and discuss the optimization of the process to realize the InP lasers with device characteristics as good as the conventional lasers fabricated on lattice-matched substrates. Section 3 describes the fabrication of the InP light emitting diodes (LEDs) on Si integrated with back-surface diffractive lenses, which will be one of the basic building blocks of the optical interconnections. In Section 4, a novel bonding process is proposed which allows the integration of optical devices on structured wafers such as actual LSI wafers, and conclusions are presented in Section 5.

2. Wafer bonding process

2.1. Bonding process and mechanism

The bonding process starts with chemical cleaning of the wafer surfaces with $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ solution, followed by rinsing in de-ionized (DI) water. After this cleaning, the surfaces show hydrophilic characteristics, which are reported to be preferable for achieving strong bonds at relatively low temperatures [22,23]. The wafers are then spin dried and their surfaces are placed in contact at room temperature under a pressure of 4 kg/cm² applied on the wafers to ensure the surface contact. The wafers adhered to each other at this stage, though the adhesion is not very strong. Finally, the wafers are annealed at elevated temperatures typically for 30 min in an H₂ atmosphere to increase the bonding strength.

The bonding mechanism has been extensively discussed for Si–Si wafer bonding [12,24] and a similar mechanism is also thought to be responsible for the InP–Si bonding. The proposed mechanism is schematically summarized in Fig. 2. First, the OH-groups are absorbed on the wafer surface during the cleaning process with $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ (Fig. 2(a)), which is thought to be an origin of the hydrophilicity. When the cleaned surfaces are brought into contact at room temperature, the wafers adhere to each other through the hydrogen bonding between the OH-groups (Fig. 2(b)). In the following heat treatment at moderate temperatures (200°C < $T$ < 400°C), water molecules ($\text{H}_2\text{O}$) start to evaporate and escape from the interface and the hydrogen bonds are replaced by bonds like InP–O–Si (Fig. 2(c)). This bond is usually stronger than the hydrogen bond, which results in increased strength at the higher temperatures. When the wafers are annealed...
at even higher temperatures \( (T > 500^\circ C) \), evaporation of phosphorus from InP and the migration of indium atoms become pronounced which can cause atomic re-arrangement at the interface (Fig. 2(d)) and the two wafers can be atomically bonded to form stronger bonds [8,14,15].

A unique feature in the case of InP–Si bonding is that the thermal expansion coefficients are different between the materials and it causes a thermal stress which may produce cracks or even separate the wafers during annealing under some conditions [9,25]. Therefore, the actual bonding mechanism could be more complicated than that described above. In addition, the bonding properties may also depend on the surface morphology and the wafer size and thickness, which makes full understanding of the mechanism more difficult. Further investigations are needed to understand the mechanism more clearly.

2.2. Optimization of bonding temperature

As suggested by the model described above, the bonding temperature is a very important parameter. Therefore, first of all, we have optimized the bonding temperature. In this work, it has been optimized in terms of (i) quality of the bonded InP crystals, (ii) bonding strength and (iii) compatibility with the device processes.

The higher limit of the bonding temperature is imposed by the degradation of InP crystal quality and Si LSI circuits. The quality of the bonded InP materials has been evaluated by measuring photoluminescence (PL) intensity. InP/InGaAsP \( (\lambda_{_{\text{pump}}}=1.3 \ \mu m) \) double-heterostructure (DH) films were bonded on Si at several temperatures and the PL intensities from the InGaAsP active layers before and after the heat treatment were measured and compared. The thickness of the InP cladding layer which determines the distance from the bonded interface to the active layer is 1.5 \( \mu m \). The PL was measured through the Si substrates using a 1.2-\( \mu m \) wavelength laser diode as the pump source. The measured PL peak intensity is shown in Fig. 3, normalized to the value obtained before the heat treatment. At temperatures above 600\(^\circ\)C, the intensity is found to decrease drastically. This indicates that the treatment temperature must be lower than 550\(^\circ\)C to maintain a good crystal quality. When DH wafers were annealed at 700\(^\circ\)C without bonding, the PL intensity exhibited no significant change. Therefore, the loss of intensity is not due to the heat treatment itself, but originates in the bonding process and could be related to the threading dislocations caused by thermal stress introduced during the heat treatment. Actually, in the cross-sectional transmission electron microscope (TEM) observation of the sample bonded at 700\(^\circ\)C, threading dislocations were clearly observed in the InP crystals near the bonded interface [26].

Additionally, bonding below 500\(^\circ\)C is preferable in terms of compatibility with Si LSI circuits, as the previously patterned Al interconnects in LSIs may be degraded at above 500\(^\circ\)C [10,11].

On the other hand, the lower temperature limit is imposed by the laser fabrication process following the wafer bonding. The formation of ohmic contacts on the InP lasers requires the annealing of the metals at about 400\(^\circ\)C, which will be described later again. Additionally, higher bonding temperatures are preferable in terms of bonding strength as the bonds usually strengthen at higher temperatures. Fig. 4 shows the measured dependence of the bonding strength on the

![Fig. 2. Proposed bonding mechanism.](image1)

![Fig. 3. Peak photoluminescence intensity from InP/InGaAsP DHs bonded on Si at different temperatures. The active layer was optically pumped through the Si substrate by a 1.2 \( \mu m \) wavelength laser and the photoluminescence emitted through the Si was measured.](image2)
treatment temperature. In this measurement, 350-µm-thick InP substrates, 5 × 10 mm², were bonded on larger Si substrates and the strength was evaluated from a shear force required to separate the wafers. As shown in Fig. 4, the bonding strength basically increases as the temperature rises, which is consistent with the mechanism explained above, although large scattering of the data is observed. We speculate the data scattering to be mainly due to the unexpected formation of voids at the bonded interface. Incompleteness of the measurement technique, such as nonuniform distribution of the applied shear force, may be an additional reason for the data scattering. Because stronger bonding will facilitate the following device fabrication, a higher temperature is also preferable from this point of view.

On consideration of these factors, the bonding temperature has been determined at 400 °C in this experiment.

2.3. Fabrication of InP edge-emitting lasers on Si

In order to examine if the bonding process is really applicable to the integration of the lasers on Si, we first fabricated the InGaAsP/InP edge-emitting lasers on Si. The laser fabrication process is summarized in Fig. 5. First of all, a DH structure was grown on a p-type (100) InP substrate by metalorganic vapor phase epitaxy (MOVPE) and was composed of a 0.2-µm InGaAs etch-stop layer, a 1.5-µm p-InP cladding layer, a 0.15-µm InGaAsP bulk active layer ($\lambda_{gap} = 1.3$ µm), a 15-µm n-InP cladding layer and a 0.1-µm n-InGaAs cap layer. The epitaxial wafer, with a typical size of 10 × 10 mm², was then stuck on a glass plate with wax for mechanical support (Fig. 5(a)). Next, the p-InP substrate and the InGaAs etch-stop layer were selectively etched to leave a thin DH film on a glass plate. The exposed surface of the p-InP cladding layer was then cleaned with $\text{Na}_{2}\text{SO}_{4}\cdot\text{H}_{2}\text{O}_{2}\cdot\text{H}_{2}\text{O}$. The surface of a Si substrate was also cleaned with $\text{H}_{2}\text{SO}_{4}\cdot\text{H}_{2}\text{O}_{2}\cdot\text{H}_{2}\text{O}$. After a DI water rinse, the wafers were spin dried and their surfaces were placed in contact under a pressure of 4 kg/cm² at room temperature (Fig. 5(b)). The wafers adhered to each other at this stage through the hydrogen bonding between the surface OH-groups.

Then, the bonded wafers were immersed in warm organic solvent to dissolve the wax from the side completely and detach the glass plate from the wafers. The wafers still remained bonded after this wax dissolving. The sample was then annealed at 400°C for 30 min in an H₂ atmosphere (Fig. 5(c)). After this annealing step, the crystal quality of the bonded DH film was evaluated by measuring PL intensity, X-ray rocking curve and etch-pit density (EPD). All the measured results indicated that the quality is good enough to realize the lasers on Si—the PL intensity as high as 90% of that before bonding, the full-width-at-half-
maximum (FWHM) of the (400) X-ray rocking curve as narrow as 35 arcsec, and the EPD of $2 \times 10^4$ cm$^{-2}$.

After bonding of the thin film, 8-μm-wide mesa stripes were formed by standard photolithography and wet etching. The active layer was slightly undercut to reduce the active width to 6 μm. Finally, AuGeNi and AuZn were evaporated and alloyed at 400°C to form n- and p-type ohmic contacts to complete the laser fabrication (Fig. 5(d)).

In this fabrication process, the 350-μm-thick InP substrate was etched away before the annealing step. When we tried to etch the substrate after annealing, the InP wafer often cracked during substrate etching, probably due to nonuniform redistribution of the thermal strain, while it hardly occurred when the wafer was bonded after substrate removal. Moreover, the flexibility of the thin film may allow it to conform to the undulations of the wafer surface, as proposed in the epitaxial liftoff process [7]. Therefore, thin film bonding is preferable and actually produces a higher yield than thick wafer bonding.

The yield of the bonding process seems to depend critically on the surface quality and preparation. For example, dust particles trapped at the interface during the bonding process lowers the yield greatly. Therefore, in this experiment, the wafers were dried and brought into contact on a clean bench with 0.3-μm particles of less than 30 counts/ft$^3$. Moreover, relatively small wafers (typically 10 × 10 mm$^2$) were used, to reduce the chances of trapping the particles between the wafers. However, the process yield was still much lower than that of conventional laser process. Other factors, such as impurities which vaporize at elevated temperatures, surface undulation and warp, can also cause void formation at the interface, which further degrades the yield. Therefore, more careful control of the wafer surface will be required to achieve a yield high enough for manufacturing, especially when larger wafers are required to be bonded.

After thinning the Si substrate down to about 100 μm, the lasers were cleaved into 300-μm-long cavities and mounted on Si heat sinks with junction-up configuration. For comparison, the same laser structure was fabricated on a p-InP substrate. The light-current ($L$–$I$) characteristics of the devices were measured at room temperature (RT) without any facet coatings. Room temperature CW operation has been achieved with these devices as shown in Fig. 6. In this figure, the $L$–$I$ curves of three lasers on Si are shown, together with those of the conventional lasers on InP for comparison. The kinks in the $L$–$I$ curves are due to multiple transverse-mode operation of the lasers with 6-μm-wide active regions. The threshold currents are about the same ($I_{th} = 39$ mA) for both the structures, which again demonstrates the high crystal quality of the bonded DH films. Moreover, maximum output powers of lasers on Si are higher than those of conventional lasers on InP. This can be attributed to the lower thermal conductivity of the Si substrates, which is one of the advantages of fabricating lasers on Si. These results indicate that the wafer bonding is a promising technique to integrate high-quality InP lasers on Si wafers.

3. InP LEDs on Si integrated with back-surface diffractive lenses

3.1. Fabrication

In order to implement the optical interconnections between Si LSIs illustrated in Fig. 1, InP surface-emitting lasers (SEls) are required to be integrated on the LSI wafers. We are thus trying to fabricate the InP SELs on Si by wafer bonding and have so far succeeded to achieve room temperature lasing operation by photo-pumping [27]. However, it is still very difficult to achieve lasing by current-injection in the InP SELs because of complexity in the device design [28]. Therefore, in this work, we have fabricated InP LEDs, instead of SELs, and demonstrated the integration of diffractive lenses on the back-surface of the Si wafers, which will be one of the basic building blocks in the interchip and/or intrachip optical interconnections.

The fabrication process is basically the same as that for edge-emitting lasers (Fig. 5) and briefly summarized in Fig. 7. First, the InGaAsP/InP double-heterostruc-
ture (DH) was grown on an n-InP substrate by MOVPE and the thin DH films were directly bonded on Si substrates (Fig. 7(a)). The thickness of the Si substrate used in this work was 300 \( \mu \text{m} \). After bonding, the active region of the LED was defined by etching the p-InP cladding and active layers to form mesa structure 20-\( \mu \text{m} \) in diameter. P- and n-type ohmic contacts were formed on InP with using polyimide as an insulator (Fig. 7(b)). Finally, the binary diffractive lenses were fabricated on the back-surface of the Si substrates by photolithography using double-view mask aligner and reactive ion etching of Si (Fig. 7(c)).

Fig. 7. Schematic fabrication process of the InP LEDs with back-surface diffractive lenses: (a) bonding of a DH thin film on a Si substrate, (b) fabrication of LED structures and (c) integration of diffractive lenses on the back-surface of the Si wafer.

Fig. 8. Pictures of the LEDs with diffractive lenses: (a) patterns of the back-surface diffractive lens and (b) simultaneous view of the front LED and back lens patterns observed with double-view microscope.

3.2. Characteristics

The output power was measured under room temperature CW operation using large-area (10 mm in di-
ameter) Ge photodetector (PD). The total power emitted through the substrate without the diffractive lens was measured by placing the Ge detector as close to the LEDs as possible, as shown in Fig. 9(a). The light output higher than 200 μW was obtained. Fig. 9(b) and (c) show the power from the LEDs (b) without and (c) with the diffractive lens, which were detected by the PD placed at some distance away from the LEDs so as to cover the solid angle of only 20°, as illustrated in Fig. 7(b). Without the diffractive lens (Fig. 7(b)), the detected power was only one tenth of the total power, which agrees well with the theoretical prediction. On the other hand, with the lens (Fig. 7(c)), about 35% of the total power was detected by the PD with the same configuration as Fig. 7(b), which indicates the LED light is collimated by the back-surface diffractive lens. Because the lens fabricated in this work is binary (two-phase) lens, the maximum diffraction efficiency is theoretically limited at about 40%. Higher collimated power will be available by using multi-level diffractive lenses, e.g., 80% with four-phase-level and 95% with eight-phase-level diffractive lenses.

Fig. 10 shows the beam size measured as a function of a distance from the diffractive lens. Although the beam is slightly divergent (with a divergent angle of about 4°), which is attributed to that the Si substrate used in this work was 20% thinner than the designed thickness, it is obvious that the directivity of the LED light is significantly improved by the diffractive lens. These results show the InP LEDs integrated with the back-surface diffractive lenses are promising devices for optical interconnects between Si LSI chips.

4. Selective-area wafer bonding

In the previous sections, we have shown that high-quality InP devices can be fabricated on pure Si substrates. However, actual Si LSI wafers, on which the devices are required to be integrated, have many structures and steps on their surfaces. In this section, we propose a bonding process which allows the integration on such structured surfaces.

Fig. 11 illustrates the proposed integration process. First, Si LSI wafers are designed and fabricated to have some vacant spaces allocated for optical devices, as shown in Fig. 11(a). Concurrently, InP DH thin
films are prepared as described previously (Fig. 11(b)) and the islands are formed in the thin films by photolithography and etching with the same pattern as the vacant spaces on the LSI wafers (Fig. 11(c)). The surfaces of both the wafers are then cleaned and the islands are aligned to the vacant spaces and directly bonded at room temperature (Fig. 11(d)). After removing the glass plate and annealing at 400°C (Fig. 11(e)), optical devices are fabricated in the DH islands by lithography and the interconnection metals are deposited and patterned (Fig. 11(f)). Since small optical devices can be defined at this step, the DH islands and the vacant spaces may be much bigger than the optical devices, which greatly facilitates the alignment at bonding in the step of Fig. 11(d). Finally, the back-surface optical elements, such as diffractive lenses and beam deflectors, can be fabricated on the back-surface of the Si wafers (Fig. 11(g)).

By using this process, we can bond to DH islands even if there are LSI patterns on the Si wafers and align the optical devices to the LSI patterns by standard photolithography. Therefore, we can integrate large number of small optical devices well-aligned to the LSI patterns, which will allow the inexpensive optoelectronic integrated circuits. Actual design of the Si LSIs with some vacant spaces (Fig. 11(a)) and integration of the optical devices on the LSIs are now under way.

5. Conclusion

Wafer bonding of InP to Si has been investigated as a key technology to integrate the optical devices on Si for interchip and/or intrachip optical interconnections. The bonding process has been optimized to allow the integration of the InGaAsP/InP DH films on Si with keeping crystal qualities good enough to make the lasers. As a result, InP edge-emitting lasers have been successfully fabricated on Si and room temperature CW operation has been achieved. In addition, InP LEDS integrated with back-surface diffractive lenses have been fabricated on Si as one of the basic building blocks in the optical interconnections. A novel bonding
process which allows the integration on actual LSI wafers has also been proposed.

Finally, it would be worthwhile to summarize the advantages of the wafer bonding over other bonding techniques, such as bonding with adhesives and flip-chip bonding. Bonding with adhesives (e.g. polyimide) has been developed and GaAs SELs were successfully integrated on Si chips [29]. However, the high thermal resistance of the adhesives causes the undesirable temperature increase of the optical devices, which will deteriorate the device performance. On the contrary, as discussed in Fig. 6, the lasers fabricated on Si with the wafer bonding technique has shown higher output powers than the conventional lasers on InP, which indicates a good heat dissipation through the bonded interface. Although metals or solders may be other candidates as adhesives with lower thermal resistance, it is opaque and not applicable to vertical optical interconnections between stacked LSIs (Fig. 1(a)). Flip-chip bonding is another promising integration technique. However, when a large number of small optical devices are required to be integrated, alignment at flip-chip bonding may become stringent and expensive. In the wafer bonding, small devices can be fabricated with conventional photolithography after grafting the InP-based materials with larger area (Fig. 11(f)), which will make the alignment very easy and inexpensive. Therefore, we believe the wafer bonding described in this paper has advantages over other bonding techniques and is very promising to realize optical interconnection between LSI chips and other optoelectronic integrations.

References