A Hybrid Current/Voltage Mode On-Chip Signaling Scheme with Adaptive Bandwidth Capability

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Abstract
This paper describes an adaptive bandwidth bus architecture based on hybrid current/voltage mode repeaters for long global RC interconnect static busses that achieves high data rates while minimizing the static power dissipation associated with current-mode signaling. An experimental adaptive bandwidth bus test chip fabricated in AMI 1.6μm Bulk CMOS indicates a reduction in power dissipation of approximately 62% over current-mode sensing and an increase in maximum data rate of 40% over voltage-mode signaling.

I. INTRODUCTION

Buffer insertion in RC dominated on-chip interconnects is often used to reduce critical path delay [1] and, given the continuing trend of increasing operating frequencies, will become essential to achieve high data rate transmission over static global busses that is often required in high-performance VLSI. To overcome the bandwidth limitations of long global busses, a signaling scheme based on current-mode sensing has been previously reported in [2]. Current sensing uses low-impedance termination to enhance the interconnect bandwidth and hence increase the maximum attainable data rate. However, the static power dissipation associated with current-sensing schemes may offset the benefit in signaling throughput.

In this paper, we propose an on-chip bus architecture based on hybrid current/voltage mode repeaters to address signal latency and throughput while minimizing the static power dissipation. The adaptive bandwidth bus (ABB) is designed to automatically increase or decrease the interconnection bandwidth given a change in bus signal activity. Since bandwidth is related to power, the ABB scheme minimizes the overall power dissipation without a penalty in maximum attainable data rate. Thus, the ABB operates in current-mode when the signal activity and the required bandwidth is high and shifts to voltage-mode operation as the data activity and the required bandwidth decreases. To demonstrate the feasibility of the proposed ABB scheme, an experimental test chip has been fabricated in AMI 1.6μm.

In section II of this paper, we propose a circuit topology for a low overhead hybrid current/voltage mode repeater. An analog implementation and experimental evaluation of the ABB is presented in section III. The limitations of this design as well as an improved all-digital ABB architecture is discussed in section IV. Finally, concluding remarks are presented in section V.

II. HYBRID CURRENT/VOLTAGE MODE REPEATER

A. Circuit Operation

A hybrid current/voltage mode repeater (HCVR) refers to a buffer that can operate in voltage or current mode, in which the “mode” of operation is simply an indication of its input impedance. Since the terminating impedance of the line determines the signal-transporting mode [2] [3], the HCVR can also be thought of as a variable input impedance buffer.

The HCVR is shown in Fig. 1 along with a driver and interconnect line. The operation of the HCVR is described as follows. When the control voltage \( V_{\text{ctrl}} \) of the input stage is below the threshold voltage of the feedback transistor, the repeater presents a high termination impedance to the line and operates as a regular full-swing voltage-mode inverter. An increase in \( V_{\text{ctrl}} \) causes the feedback transistor to turn on and the repeater to operate as a self-biased inverter, thus lowering the termination impedance of the line.

B. Measurement Verification

A test chip fabricated in AMI 1.6μm CMOS process was used to validate the operation of the HCVR. Fig. 1 shows the test line used for measurements. The line resistance and capacitance are approximately \( R_T=375\Omega \) and \( C_T=1.43\text{pF} \), respectively.

Shown in Fig. 2 are the measured voltage waveforms of the HCVR under different \( V_{\text{ctrl}} \) biases. The rise time at the HCVR input (i.e. INh) is measured to be 2.96ns for \( V_{\text{ctrl}}=0\text{V} \) and 1.35ns for \( V_{\text{ctrl}}=5\text{V} \), a reduction of 55%. Similarly, the overall propagation delay from IN to OUT is 2.45ns for \( V_{\text{ctrl}}=0\text{V} \) and 2.04ns for \( V_{\text{ctrl}}=5\text{V} \), a 17% delay reduction.

The maximum bandwidth or NRZ data rate of the HCVR for several \( V_{\text{ctrl}} \) voltages is depicted in Fig. 3. In order to characterize the bandwidth performance of the interconnection and low-to-high swing conversion circuit, measurements were taken at the input (i.e. INh) and output (i.e. OUT) nodes of the HCVR, respectively. The maximum bandwidth of the interconnection, obtained via 1/rise-time measurements at INh, indicate an increase of nearly 400Mb/s over the \( V_{\text{ctrl}} \) range. However, the maximum NRZ data rate...
measured at the output node (i.e. OUT) was limited to 660Mb/s, above which the pulses began to distort due to the speed limitation of the low-to-high swing circuit. Although in the present design the low-to-high swing conversion consists of a couple cascaded inverters, a more advanced process with faster devices is likely to remove this limitation.

III. ANALOG ADAPTIVE BANDWIDTH BUS

A. Architecture

The ABB scheme consists of HCVR buffers inserted along an interconnect line with a control unit that senses input data activity, as depicted in Fig. 4. The analog control unit of the ABB scales with device feature size, and can be shared among multiple bus lines to minimize circuit area overhead. The functional block diagram of the control unit is shown in Fig. 5a. It consists of a transition detector (TD), a charge pump (CP) and a lone pulse detector (LPD).

The control unit of the ABB essentially converts data switching activity into a voltage $V_{ctrl}$ that is used to set the operation mode of the HCVR (i.e. current or voltage mode). This is done via the TD and CP shown in Fig. 5b. The TD senses the input data stream forcing the CP to charge the control line voltage ($V_{ctrl}$) when there is an input signal transition, or discharge in the absence of thereof. Thus, the required bus bandwidth is determined by the data switching activity.

As shown in Fig. 5a, the LPD operates in parallel with the CP to ensure correct data transmission given the onset of a lone input pulse – i.e. a narrow pulse preceded by a long period of inactivity. Since in the absence of data transitions $V_{ctrl}$ is discharged low to minimize power dissipation, the ABB must ensure that $V_{ctrl}$ is pulled high before the pulse is launched in the repeater chain so as to allocate the required interconnect bandwidth. The LPD, shown in Fig. 5c, ensures this condition by forcing $V_{ctrl}$ high via large PMOS transistors to update the HCVR operation to current-mode. It should be pointed out that, since data cannot be launched prior to updating $V_{ctrl}$, the update-time of the LPD represents the worst-case processing delay of the ABB. To further reduce the processing delay of the ABB, an improved all-digital architecture is proposed in section IV.

Notice that two additional bias voltages $V_{TH}$ and $V_{down}$, are designed into the LPD and CP to externally force $V_{ctrl}$ high or low. For instance, by setting $V_{TH}=V_{dd}$ and...
$$V_{\text{down}}=\text{GND}, \ V_{\text{ctrl}} \text{ will remain pulled high regardless of input data transitions} – \text{a condition used to test the repeater chain under current-mode (CM) operation. Conversely, reversing the bias voltages enforces voltage-mode (VM) operation (i.e. } V_{\text{TH}}=\text{GND} \text{ and } V_{\text{down}}=V_{\text{dd}}).$$

### B. Experimental Results

Shown in Fig. 6 is a photograph of the test chip fabricated in AMI 1.6um. Due to the small die area, poly interconnects were used to model the effect of long RC wires. Measured waveforms shown in Fig. 7 depict the operation of the ABB. Fig. 7a shows an arbitrary input data stream (IN) and control voltage ($V_{\text{ctrl}}$), which reacts to the input signal activity. In the absence of transitions, the CP block discharges $V_{\text{ctrl}}$ low within approximately 36ns, whereas the LPD updates $V_{\text{ctrl}}$ high on the onset of a pulse within 2ns. Notice that the fast update time is necessary to allocate bus-signaling bandwidth before data is launched. Fig. 7b shows the waveforms at the output node (OUT) indicating correct data detection.

Shown in Fig. 8 is a comparison of the power dissipation versus data rate performance for current-mode (CM), voltage-mode (VM) and adaptive-mode (ABB) signaling schemes. The measured results are based on a test line with four uniformly spaced repeaters dividing an interconnect line into wire segments of $R_T=436\Omega$ and $C_T=1.65pF$ each. At $V_{\text{dd}}=5V$ (Fig. 8a), the ABB scheme achieves the same maximum data rate as the CM scheme (approximately 40\% higher than VM signaling), while minimizing the power dissipation by nearly 62\% over the CM bus when the activity rate is low. Reducing the supply voltage to $V_{\text{dd}}=3V$ (Fig. 8b) yields similar improvements in relative performance for the ABB scheme – approximately 50\% increase in signaling rate over the VM bus and 63\% reduction in power over the CM bus. Furthermore, a comparison between the ABB scheme at $V_{\text{dd}}=3V$ and the VM bus at $V_{\text{dd}}=5V$ indicates nearly 2.5x reduction in power dissipation with only 4.5\% penalty in maximum data rate (i.e. 420Mb/s /440Mb/s).

It is worthwhile noting that the discharge time of $V_{\text{ctrl}}$ determines the data rate for which the ‘Adaptive’ and ‘CM’ curves in Fig. 8 merge, and should be considered to further improve the power dissipation performance of the ABB. Since $V_{\text{ctrl}}$ sets the operation of the bus in current or voltage mode, the slower it discharges the longer it remains in current-mode dissipating static power. Thus, reducing the $V_{\text{ctrl}}$ discharge time yields a reduction in power dissipation at higher data rates, effectively shifting the ‘Adaptive’ curve in Fig. 8 to the right.

In the present design, a capacitance ($C_{\text{ctrl}}=1.5pF$) was added to the output of the CP in Fig. 5b to regulate the control voltage ($V_{\text{ctrl}}$). However, experimental results indicated that this is not necessary. In fact, the addition of $C_{\text{ctrl}}$ causes the discharge time to increase, which limits the improvement in power dissipation of the ABB scheme at higher data rates.

In general, an important advantage of CM sensing over VM signaling is that its dynamic power dissipation component can be significantly reduced as a result of smaller voltage swings in the interconnect [2]. This can be inferred from Fig 8 by noting that the slope at which the power increases with increasing data rates is smaller for the CM bus. For instance, at $V_{\text{dd}}=5V$, the measured change in current is $24\mu A/Mb/s$ for CM signaling and $55\mu A/Mb/s$ for VM signaling – a reduction of 56\%. Thus, at higher operating frequencies, the power dissipation of full-swing VM signaling is likely to become more dominant.

### IV. Digital Adaptive Bandwidth Bus

One of the drawbacks in the analog implementation of the ABB is that the bus input-to-output propagation delay varies with $V_{\text{ctrl}}$ – as the bandwidth of the line is proportional to
This uncertainty in propagation delay and data arrival time with respect to the global clock boundaries may cause detection errors at the receiving end of the bus. In order to ensure correct data detection, the digital ABB implementation uses a binary or digital control line to set the bandwidth of the bus lines. Thus, in the event of data transitions, $V_{ctrl}$ is set to logical level HI; and in the absence of data transitions $V_{ctrl}$ is set to logical level LO. Since data transitions are sent across the bus lines only when the control voltage is set to the appropriate voltage level, the propagation delay remains constant.

The architecture of the digital adaptive bus is shown in Fig. 9. It consists of a small FIFO of depth $C_p+1$ clock cycles, a digital transition detector, a control line and the hybrid voltage/current mode repeaters. The input to the control line (Cin) sets the operation of the hybrid repeaters in either voltage or current-mode. In the event of input data transitions (Din[0], Din[1],…Din[N]), the transition detectors activate the control line to set the bus lines in CM operation mode. Similarly, in the absence of data transitions, the bus lines are set to VM operation mode. Specifically, if the data Din[0:N] does not change for $C_p$ clock cycles, the bus lines automatically shift to VM operation to reduce the static power dissipation. In order to minimize circuit overhead, each control line is shared among $(N+1)$ bus lines.

The bus operation in each clock cycle for an arbitrary input data sequence is shown in Fig. 10 (from hereon a clock cycle refers to the system sampling time). In this example, the data is sampled at both positive and negative edges of the clock. For simplicity, we assume that two bus lines Din[0] and Din[1] share the same control line C0. As shown in Fig. 10, the input data is delayed by $C_p$ clock cycles to allow for the transition detectors and control line to update the repeater’s mode of operation. The minimum required $C_p$ is given by the overall processing delay of the path determined by the transition detectors and control line. Since the control line is identical to the bus lines and continuously operates in CM, only the first repeater of the bus lines needs to be updated before the delayed input data (Bin[0:N]) can be launched. As the control signal C0 propagates, it updates the subsequent repeater stages of the bus lines, similar to a domino effect. The importance of this is that the latency of the processing delay from CM-to-VM or vice-versa is significantly reduced. In Fig. 10, $C_p$ is assumed to be two cycles long. On the falling edge of the control signal C0, the line switches to VM after approximately two cycle delays, indicated by the shaded regions. Notice that the data bus lines switch to CM operation whenever there is an input transition, and remains in VM operation in the absence of transitions for more than $C_p$ cycles.

V. CONCLUSIONS

An adaptive bandwidth bus architecture based on hybrid current/voltage mode repeaters for signaling across long global RC interconnects has been presented to minimize the static power dissipation inherent to current-mode sensing while achieving high data transmission rates. Measurement results indicate a 62% improvement in static power dissipation over CM sensing techniques while achieving 40% increase in maximum data rate over VM signaling. A comparison of the ABB and VM signaling schemes operating at Vdd=3V and Vdd=5V, respectively, shows that the ABB dissipates nearly 2.5x less power with only 4.5% penalty in maximum data rate.

REFERENCES