Impacts of Hole Trapping on the NBTI Degradation and Recovery in PMOS Devices

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1. Introduction
Negative bias temperature instability (NBTI) in PMOS devices represents a major reliability concern in modern CMOS technologies. NBTI phenomenon results in threshold voltage (Vth) shift and drain current degradation, and becomes more severe as gate dielectric is thinned down [1]. Moreover, nitrogen incorporation in the gate dielectric may further exacerbate the issue [2]. In general, NBTI is attributed to the generation of interface states and fixed charges during stressing [3][4]. Recently, the recovery of Vth shift after the removal of the bias-temperature stress has been observed and characterized [5]-[9]. It was speculated that the recovery was mainly related to the re-passivation of interface states by hydrogen that occurred after the stress was stopped [5][6], though more recently it was shown that de-trapping of holes could also be responsible for this phenomenon [8][9]. Furthermore, a clear picture regarding the channel length dependence of this behavior is still lacking, and few efforts were devoted to clarifying the difference in recovery behavior among different gate dielectrics such as pure oxide and SiON. In this work, we addressed these issues by characterizing the devices with ultra-thin gate dielectrics (EOT < 2 nm).

2. Experimental
Dual-gate p- and n-channel MOSFETs were fabricated using a standard 0.13 micron CMOS twin-well technology. Three types of gate dielectric, i.e., thermal oxide, nitrided oxide, and N/O stack, were characterized and compared in this work. Equivalent oxide thickness (EOT) of the test devices was determined using a capacitance-voltage (CV) method that took into account both the quantum mechanical and the poly gate depletion effects. The bias-temperature stress (BTS) was performed at 150 °C under a gate bias ranging form -2 ~ -2.5 V for 5000 sec, with all other electrodes (S/D and well) grounded. After the stressing, the devices were relaxed at either 150 °C or room temperature, as shown in Fig. 1. For the latter case, cooling of devices took about 20 minutes. The recovered Vth was defined as the magnitude of the Vth shift that occurred during the relaxation period.

3. Results and Discussion
Figure 2 shows the Vth shift as a function of stress time for samples having EOT of 1.6 nm. As can be seen in the figure, the pure oxide exhibits less Vth shift than the other two splits, indicating that the introduction of nitrogen in the gate dielectric aggravates the NBTI. Furthermore, the pure oxide also shows more Vth recovery than the other two splits, indicating that the introduction of nitrogen in the gate dielectric aggravates the NBTI. This is mainly ascribed to the reduced oxide field during stress [8]. The magnitude of Vth shift increases with decreasing channel length, consistent with a previous report [3], implying that the hole concentration along the channel during stress plays a role in affecting the NBTI. Still, N/O stack devices exhibit higher NBTI immunity than the nitrided oxide devices.

Figure 4 shows the amount of Vth recovery as a function of channel length for devices relaxed at room temperature for 48 hours after the BTS. Note that the results for pure oxide are not shown, since only negligible recovery is found. For the other splits, recovery behavior is clearly detected, and becomes more pronounced for devices with shorter channel length. This means that, in practical application, the devices’ Vth may recover even after the circuit is turned off when N/O or nitrided oxide is used. Interestingly, although the N/O stack split exhibits less Vth shift during BTS than the nitrided oxide one (Figs. 2&3), in Fig. 4 it is observed that the use of N/O stack results in a larger amount of Vth recovery.

To gain insights into the observed phenomena, charge-pumping characterization was employed. In order to avoid the influence due to gate leakage, samples with thicker gate dielectric (EOT ~ 1.9 nm) were used. Figure 5 shows the results for a device with nitrided oxide. It is seen that the Icp remains unchanged after relaxation at room temperature for 26 hours, albeit visible Vth shift (~ 2 mV) is detected. This indicates that the generated interface states play only a minor role in the recovery process at room temperature. Figure 6 depicts the evolution of Vth and Icp at the stress temperature. It is seen that most Vth recovery occurs within the first 500 sec, while a decrease in Icp is also observed, implying that the re-passivation of interface states indeed takes place. Nevertheless, its contribution to the Vth recovery is very small, as shown in Fig. 7. This indicates that the de-trapping of trapped holes during the relaxation period is mainly responsible for the recovery phenomenon at the stress temperature. It is also believed
that the device with N/O stack would exhibit similar behavior. Unfortunately, we lack the devices with EOT thick enough for charge pumping characterization.

Figure 8 shows the evolution of Vth and Icp at the stress temperature for a device with pure oxide (EOT = 2 nm). As can be seen in this figure, Icp remains essentially constant after the stress, indicating that the re-passivation of interface states is correlated with the existence of nitrogen incorporated in the gate dielectric. Although Vth recovery is also observed, its value is smaller than the N/O stack and nitrided oxide counterparts. Note also that the Vth recovery behavior becomes indiscernible when the relaxation takes place at room temperature.

Based on the results shown above, we conclude that de-trapping of trapped holes in the gate dielectric is the primary mechanism responsible for the recovery phenomenon. For ultra-thin oxide, the trapped holes can easily tunneled back to the channel [10] at elevated temperature, thus the recovery is no longer detectable when the device has already cooled down. When nitrogen is introduced into the dielectric, however, the trapped holes are likely to stay in the nitrogen-related defects for a longer period. After removing the stress, de-trapping of holes is responsible for the recovery phenomenon. Figure 9(a) shows the band diagram to explain the recovery behavior for the N/O gate dielectric [11]. Specifically, after the BTS, the trapped holes gradually return to the substrate, so the device’s subthreshold characteristics recover. As shown in Figs. 2 and 3, the N/O stack sample depicts more pronounced recovery phenomenon than the nitrided oxide sample. This is primarily due to a higher N concentration and the existence of an interfacial oxide layer that would block the trapped holes in the dielectric from being easily tunneling out of the dielectric.

The data shown in Fig. 4 indicate that the recovery phenomenon is more profound as the channel becomes shorter. This could be explained by the following two reasons: (1) The data shown in Fig. 3 imply that the density of trapped holes in devices increases with decreasing channel length, so the de-trapping events of holes after BTS would also increase in the short-channel devices. (2) The band-diagrams shown in Fig. 9(b) indicate that, due to the opposite electric field in the oxide, the trapped holes over the channel regions have a lower probability of returning to the substrate than those over the S/D extension regions.

4. Conclusions

In summary, we have shown that Vth recovery could occur at room temperature for PMOS devices with N/O stack gate dielectric and nitrided oxide. The recovery phenomenon becomes more significant as the channel length is shortened. Our results of charging pumping characterization unambiguously indicate that the de-trapping of holes plays a major role in the recovery process. We have also found that the re-passivation of interface states during relaxation is related to the nitrogen incorporation.

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References


Fig.1 Experimental scheme for stressed devices relaxed at (a) the stress temperature and (b) room temperature.
Fig. 2 Vth shift as a function of stress time.

Fig. 4 Recovered Vth at room temperature as a function of channel length. The measurements were performed 48 hours after the BTS.

Fig. 5 Results of charge pumping measurements performed at room temperature.

Fig. 6 Evolution of Vth and Icp during stress and relaxation periods at the stress temperature. The device has nitried oxide with EOT of 1.9 nm.

Fig. 7 Recovered Vth as a function of channel length. The measurements were performed 48 hours after BTS.
Fig. 8 Evolution of Vth and Icp during stress and relaxation periods at the stress temperature. The device has pure oxide with EOT of 2 nm.

Fig. 9 Band diagrams at (a) channel and (b) S/D extension regions (Vg = 0).