3-D Simulation of Strained Si/SiGe Heterojunction FinFETs

S. T. Chang\textsuperscript{a,}\textsuperscript{*}, B.-C. Hsu\textsuperscript{b}, S. H. Hwang\textsuperscript{b}

\textsuperscript{a} Department of Electronic Engineering, Chung Yuan Christian University, Chung-Li, Taiwan, R. O. C. E-mail: stchang@cycu.edu.tw

\textsuperscript{b} Department of Electrical Engineering and Graduate Institute of Electronics Engineering, National Taiwan University, Taipei, Taiwan, R. O. C.

The 3-D structure and the possible process flow of the proposed strained Si/SiGe FinFETs are given in Fig. 1 and Fig. 2 (a)-(e), respectively. The strained Si surrounds the embedded SiGe body, and the exact strain partition between the tensile strained Si and the compressively strained SiGe depends on the physical dimensions and thermal process of the device. For convenience, a fully strained Si and a fully relaxed SiGe are used in the simulation with the assumption that the strained-Si is thin enough or the strained Si/relaxed SiGe is in the metastable state due to the low thermal budget. A channel doping of $10^{16}$ cm$^{-3}$, dual polysilicon gate (n$^+$ for NMOS, p$^+$ for PMOS), 1.5 nm gate oxide, abrupt source/drain-to-channel junctions, and a Si$_{0.8}$Ge$_{0.2}$ body with fixed 5 nm surrounding Si are used in the 3-D simulation [1]. The mobility enhancement factors of 1.7 and 2 are used for electrons and holes in the strained Si respectively, while the SiGe body has a lower electron mobility of 0.25x and a lower hole mobility of 0.6x as compared to control Si. The type II band alignment of strained Si/SiGe heterojunction can have the electron confinement in the conduction band of the strained Si, and the hole confinement at strained Si/SiGe heterojunction (Fig. 2(f)).

The control device has a higher electron concentration at fin center for the subthreshold and threshold bias, but has a surface conduction channel close to the Si/oxide interface at over threshold bias, while the strained Si/SiGe device has a conduction channel in the strained Si at all three bias conditions (Fig. 3). The conduction channel closer to the Si/oxide interface for the strained Si/SiGe device at the subthreshold bias yields a better gate control, and thus a smaller subthreshold swing as compared to the control device (Fig. 4). The smaller fin width can make a channel closer to the Si/oxide interface and thus yields a smaller subthreshold swing for both devices (Fig. 4). The subthreshold swings of both devices decrease with increasing channel length (Fig. 4). The drain potential decay length $L_D$ (Fig. 5) [2] increases as the fin width increases. The increase of drain-induced barrier lowering (DIBL) due to the increasing $L_D$ yields a negative $V_T$ shift at large fin width for both devices. Both devices have a $V_T$ roll-off at short channel, but strained Si/SiGe device has a slightly smaller roll-off. The strained Si/SiGe device has a lower (more negative) threshold voltage (Fig. 6) than the control device due to the lower conduction band edge in the strained Si than that in SiGe (Fig. 2(f)). The transconductance ($g_{m}$) of the strained Si/SiGe device is larger than that of the control device, and has a smaller roll-off at large gate voltage ($V_{GS}>0.2$ V) for different channel length (Fig. 7) and fin width (Fig. 8). The peak $g_{m}$ enhancement is more significant at small channel length (the inset of Fig. 7). The larger fin width yields a larger $g_{m}$ due to the smaller channel resistance (Fig. 8). For the PMOS, the hole distributions of both devices have peaks at the fin center and form buried-channel conduction path in the subthreshold region. The on-state, the strained Si/SiGe device has two conduction channels at the Si/oxide interface (surface channel) and the strained Si/SiGe interface (buried channel), while the control device has only a surface channel at Si/oxide interface (Fig. 9). The buried channel yields the inferior subthreshold swing of the strained Si/SiGe device as compared to the control device (Fig. 10). For both devices, the larger fin width has the conduction path away from Si/oxide interface in the subthreshold region, and yields larger subthreshold swing (Fig. 11). Due to the band offset at the strained Si/SiGe heterojunction, the hole inversion layer can be formed at the less negative gate bias (Fig. 11) and the strained Si/SiGe device has a more positive $V_T$. A worse threshold voltage roll-off of the strained Si/SiGe device is observed channel length and fin width decreases (Fig. 12). This novel strained Si/SiGe FinFET with the enhanced carrier mobility and heterojunction confinement is demonstrated with greatly improved performance for NMOS by 3-D simulation. The PMOS is not improved as much as NMOS due to the buried channel at the Si/SiGe heterojunction.

Fig. 1 The strained Si/SiGe FinFET structure. (a) Three dimensional schematic diagram. The spacers between source/drain are not shown in order to reveal the fin structure. (b) Cross-section view along A-A’.

Fig. 2 (a-c) The proposed fabrication flow of strained Si/SiGe FinFET. (f) Type II band alignment of strained Si/SiGe heterojunction.

Fig. 3 Electron distribution along the A-A’ cross-section under three different bias conditions for (a) control and (b) strained Si/SiGe NMOS. Bias conditions are (i) subthreshold region: $V_{GS}-V_T = -0.1V$ (ii) at threshold: $V_{GS}-V_T = 0V$ (iii) over threshold region: $V_{GS}-V_T = 0.3V$.

Fig. 4 Dependence of subthreshold swing on fin width $T$ and channel length $L_g$. A narrower fin width shows lower subthreshold swing. A shorter channel length shows higher subthreshold swing. The subthreshold swing is improved in the strained Si/SiGe device as compared to the control device.

Fig. 5 $L_g$ dependence on DIBL. Larger $L_g$ has larger barrier lowering and yields a more negative $V_T$; $H$ is the fin height.

Fig. 6 Threshold voltage roll-off characteristics. Strained Si/SiGe device has a slightly smaller roll-off.

Fig. 7 NMOS transconductance for the strained Si/SiGe and control devices. Larger $g_m$ enhancement and smaller $g_m$ roll-off at large $V_{GS}$ are observed in the strained Si/SiGe device. The $g_m$ is normalized by the effective device width ($2H+T$).

Fig. 8 NMOS transconductance for the strained Si/SiGe and control Si devices with different fin widths. The inset is the peak $g_m$ vs fin width. The $g_m$ is normalized by the effective device width ($2H+T$).

Fig. 9 Hole distribution along the A-A’ cross-section under three different bias conditions for (a) control and (b) strained Si/SiGe PMOS. Bias conditions are (a) subthreshold region: $V_{GS}-V_T = -0.3V$. (b) at threshold: $V_{GS}-V_T = -0.1V$ at threshold region: $V_{GS}-V_T = -0V$ (c) over threshold region: $V_{GS}-V_T = 0.3V$.

Fig. 10 Dependence of subthreshold swing on fin width $T$ and channel length $L_g$. The strained Si/SiGe device shows higher subthreshold swing than the control device.

Fig. 11 The band diagram of the strained Si/SiGe device and control device. Due to band offset at Si/SiGe heterojunction, the hole inversion layer can be formed at less negative gate voltage.

Fig. 12 Dependence of threshold voltage on fin width $T$ and channel length $L_g$. The strained Si/SiGe device has a slightly larger roll-off.