Buried Oxide Thickness Effect and Lateral Scaling of SiGe HBT on SOI Substrate

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The devices fabricated on SOI can improve the RF and reduce cross-talk for mixed signal circuits [1]. The buried oxide thickness used in SOI devices can accommodate the BiCMOS process and are mostly used in high-speed and high power applications. IBM group [1, 2] has demonstrated that a SiGe heterojunction bipolar transistor (HBT) on SOI substrate with a fully depleted collector can offer higher base-collector breakdown voltage, higher Early voltage and better BVCEO\textsuperscript{fT} tradeoff through experiment and simulation. In this paper, the key design device parameter of SOI such as the buried oxide thickness is studied by 2-D device simulator DESSIS [3].

The schematic structure of a Si\textsubscript{1-x}Ge\textsubscript{x} HBT on SOI substrate is given in Fig. 1. The bulk device for comparison has a collector thickness of 0.3\textmu m and a heavily doped n\textsuperscript{+} reach-through region. The buried oxide thickness is varied from 0.06 to 0.2\textmu m. The base width is about 75 nm and the emitter size is 0.14\textmu m\times10\textmu m. Doping profile and Ge mole fraction follow the secondary ion mass spectroscopy (SIMS) data of ERSO baseline SiGe HBT process [4]. The emitter, base, and collector doping are 10\textsuperscript{20}, 10\textsuperscript{18}, and 10\textsuperscript{17} cm\textsuperscript{-3}, respectively. The larger Early voltage \textit{V}_E is observed in SOI device due to lower base-collector junction capacitance \textit{C}_BC (Fig. 2). Early voltage and \textit{C}_BC as a function of the buried oxide (BOX) thickness are shown in Fig. 3. \textit{C}_BC is almost invariant as the buried oxide thickness is thicker than 0.08\textmu m, which is smaller than that of bulk device. The base open breakdown voltage (BVCEO) increases with increasing BOX thickness (Fig. 4). The electric field at B-C junction decreases as BOX thickness increases, due to the extra voltage drop in the BOX (Fig. 4). The impact ionization rate is a strong function of electric field. The lower electric field of the SOI devices indicates the higher breakdown voltage BVCEO. As BOX thickness increases, \textit{f}_T starts to decrease rapidly and then decreases slightly (Fig. 5). This is due to \textit{C}_BC almost keep the same value as BOX thickness is larger than 0.08\textmu m. This behavior is confirmed by SPICE simulation. BOX thickness affects the collector-substrate capacitance \textit{C}_{CS}. Effective \textit{C}_{CS} is a series of \textit{C}_{OX} (BOX capacitance) and \textit{C}_{CS,SOI} (BOX –substrate capacitance). Is keeps the same in all BOX thickness devices and \textit{C}_{CS} decreases as BOX thickness increases. SPICE simulation shows that variation of \textit{C}_{CS} do not affect cutoff frequency seriously. As BOX thickness increases, \textit{f}_{max} decreases because of the increase of \textit{C}_{BC} (Fig. 6). The \textit{C}_{BC} increases due to the \textit{C}_{CS,SOI} and then decreases as BOX thickness increases. SPICE simulation demonstrated that variation of \textit{C}_{CS} affects \textit{f}_{max}. The variation of \textit{C}_{CS} is from variation of \textit{C}_{CS,SOI} due to change of BOX thickness.

Given BOX thickness of 0.15\textmu m and collector doping of 10\textsuperscript{17} cm\textsuperscript{-3}, both \textit{f}_T and \textit{f}_{max} decrease as \textit{L}_{col} decreases (Fig. 7). The increase of the lateral depletion region with increasing \textit{L}_{col} can be responsible for this result. However, the increase of \textit{L}_{col} can decrease the peak electric field (Fig. 8) in the devices, and thus increases the BVCEO (Fig. 9). The tradeoff between \textit{f}_T/\textit{f}_{max} and BVCEO exists due to the \textit{L}_{col} [1, 2]. If \textit{f}_T/\textit{V}_{CEO} product is used as a figure of merit, the maximum value is obtained at \textit{L}_{col} =0.15\textmu m. Given \textit{L}_{col} of 0.15 \textmu m and collector doping of 10\textsuperscript{17} cm\textsuperscript{-3}, \textit{f}_T decreases as BOX thickness increases while \textit{f}_{max} shows the opposite trend. However, the increase of BOX thickness (\textit{T}_{ox}) can decrease the peak electric field (see Fig. 4) in the devices, and thus increases the BVCEO. The tradeoff between \textit{f}_T/\textit{f}_{max} and BVCEO exists due to the BOX thickness. If \textit{f}_T/\textit{V}_{CEO} product is used as a figure of merit, the maximum value is obtained at \textit{T}_{ox} = 0.1\textmu m under fixed \textit{L}_{col} condition.

In summary, as compared to bulk SiGe HBTs, the SiGe HBTs on SOI substrates have a higher Early voltage, maximum oscillation frequency, and breakdown voltage. Buried oxide (BOX) thickness effect and the lateral distance between collector and reach-through region of SiGe HBT on SOI substrates are investigated. A SiGe HBTs on SOI substrates with larger buried oxide thickness can achieve a higher BVCEO and \textit{f}_{max} with a comparable \textit{f}_T and \textit{V}_E. Optimal design of The BOX thickness and \textit{L}_{col} for SiGe HBTs on SOI has been studied.

Fig. 1 Schematic of a SOI SiGe HBT. $L_{col}$: the distance from the n+ reach-through to the edge of the intrinsic base. $T_{ox}$: buried oxide thickness.

Fig. 2 Output characteristics of bulk and SOI SiGe HBTs. The base current varies from 0.01µA/µm to 0.1µA /µm. Early voltage of SOI device is larger for than that of bulk device at $I_{B}=0.1µA /µm$

Fig. 3 Early voltage and $C_{BC}$ vs oxide thickness. $C_{BC}$ is almost not change as oxide thickness increases. $V_A$ decreases slightly as oxide thickness increases.

Fig. 4 $BV_{CEO}$ and maximum electric field at B-C junction vs oxide thickness. $BV_{CEO}$ increases as oxide thickness increases. Peak electric field decreases as oxide thickness increases.

Fig. 5 Cutoff frequency and $C_{BC}$ vs oxide thickness. Cutoff frequency and $C_{BC}$ both decrease as oxide thickness increases.

Fig. 6 $f_{max}$ and $C_{cs}$ vs oxide thickness. $f_{max}$ increases as oxide thickness increases while $C_{cs}$ decreases as oxide thickness increases.

Fig. 7 $f_T$ and $f_{max}$ vs $L_{col}$. Both $f_T$ and $f_{max}$ decrease with oxide thickness increasing.

Fig. 8 Lateral electric field distribution with three different lengths of $L_{col}$. Buried oxide thickness is fixed as 0.15 µm.

Fig. 9 Base open breakdown voltage ($BV_{CEO}$) as function of $L_{col}$. $BV_{CEO}$ increases with increasing $L_{col}$. 