Native oxide free polycrystalline/single crystal Si interface obtained by in situ cleaning: effects on the electrical performances of polysilicon emitter transistors

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Abstract

We compare polysilicon emitter bipolar transistors fabricated by using different treatments of the interface between single crystal and polycrystalline Si (polysilicon) in the emitter region. One of the treatments consisted in an in situ cleaning of the silicon surface performed in the deposition chamber prior to the polysilicon deposition, resulting in an oxide free interface. A detailed structural and electrical characterization of transistors with and without an oxide free interface is presented. It is shown that, even if common emitter current gain decrease is observed, a strong improvement of base resistance and breakdown voltage can be achieved, while maintaining noticeable high frequency characteristics.

1. Introduction

Adoption of polysilicon into silicon bipolar integrated circuit processing has given considerable improvements in packing density and switching performance [1]. One main feature of these devices is that polysilicon can be used as diffusion sources for the doping of emitter and of intrinsic base layer. Moreover, self-alignment of the emitter and base contact regions can be easily achieved. One of the problems of scaling conventional bipolar transistors is the decrease of the common emitter current gain, which occurs as the vertical dimension shrinks [2]. However, in the case of an n–p–n transistor, by intentionally forming a thin oxide layer at the polysilicon/single crystal Si interface in the emitter region, it is possible to obtain large gain improvements [3]. This is attributed to the larger tunneling probability of the electrons through this oxide layer compared to holes [4]. In that case it is possible to raise again base doping concentration, i.e. to decrease base resistance, while maintaining a reasonable current gain. However, all of the above findings refer to conventional LPCVD polysilicon deposition systems, which at the moment do not allow a good control of this interface. In fact, during the air break after the cleaning of the surface and the emitter polysilicon deposition, usually an oxide film

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grows on the Si surface. After the deposition, at typical temperatures required for doping diffusion, this oxide film can break up, and the poly-Si layer starts to realign to the same substrate orientation. The lateral size of the realigned regions is of the order of 200 nm, i.e. of the order of the emitter size. For this reason this phenomenon could affect the uniformity of the electrical characteristics of different devices of a same wafer. At the moment it is not clear what happens if one completely eliminates the interfacial oxide. In this paper we report the results of the characterization of a new process scheme for emitter formation, that is based on the complete removal of the interfacial oxide, obtained by means of an in situ cleaning.

2. Experimental

Three types of polysilicon emitter bipolar transistors were fabricated by using identical standard processing up to the surface treatment of the (100) silicon wafers prior to the polysilicon emitter deposition. To remove native oxide, all of the wafers were ex situ cleaned, i.e. dipped for 40 s, in HF:H₂O, 1% diluted, immediately before the introduction into the polysilicon deposition chamber. Reference devices were fabricated by depositing, at 610°C, 130 nm thick undoped polysilicon in a conventional LPCVD hot wall horizontal reactor, directly after the ex situ Si surface cleaning. Because of the air break, prior to the introduction in the polysilicon deposition chamber, a thin oxide film regrows on the silicon surface. After deposition, to break the interfacial native oxide, the wafers were first pre-annealed at 1025°C for 30 s. They were and then doped by ion implantation of As at an energy of 30 keV to a dose of $6 \times 10^{15} \text{cm}^{-2}$.

The alternative emitter formation process consisted in depositing polysilicon layers, in situ doped with As. The system used was a single wafer high temperature polysilicon deposition CVD equipment (Centura® Poly). After the ex-situ HF cleaning of the Si surface, the wafers were introduced in a load-lock chamber, at room temperature, and then into the deposition chamber, already set at deposition temperature of 660°C. A group of these wafers was first subjected also to an in situ high temperature H₂ bake, used to clean the Si surface from the residual native oxide, and then to the polysilicon deposition. We will refer to these samples as with bake. A second group of wafers was directly subjected to the in situ As doped polysilicon deposition without any preliminary in situ surface cleaning (without bake samples). All of the wafers (reference, without and with bake) were then annealed, in a rapid thermal process (RTP) annealer, at 965°C for 30 s, to activate and diffuse the dopant, and then followed a standard metallization procedure.

Non-patterned test wafers, which had received identical interface treatments and emitter processing, were used for the transmission electron microscopy (TEM) and other structural investigations. These samples were also capped with ~2 nm of chemical silicon dioxide, to
avoid arsenic evaporation during the annealing process. Samples in cross section along (100) planes were prepared by mechanical thinning, followed by Ar⁺ ion milling, for TEM observations. These were examined using a 2010 JEOL TEM operating at 200 kV accelerating voltage. Detailed electrical measurements were carried out on transistors on wafer, by using two 236 Keithley source/measure units and a Keithley 6512 electrometer for DC measurements, and a HP network analyzer to measure S-parameters in the 0.05–20 GHz frequency range.

3. Results and discussion

Fig. 1 shows the cross-sectional transmission electron micrographs of the interface region in the three different final samples. Fig. 1(a) shows the reference sample, with the deposited silicon on the top of the figure, and the substrate on the bottom. The not uniform bright band separating the silicon substrate from the deposited layer, represents the interfacial silicon oxide, probably regrown during the elapsed time before the deposition, and during the introduction in the high temperature deposition chamber. The bright contrast is due to the differences in the atomic scattering factor between the silicon and the silicon oxide. As it is possible to see in Fig. 1(a) the deposited layer is a single crystal material with the same crystallographic orientation as the underlying silicon, this being deduced from the micrograph contrast, that is the same in the two regions. The realignment of the deposited polysilicon suggests that the interfacial oxide, under heat treatment at 1025°C for 30 s, broke up. The polycrystalline regions in direct contact with the underlying crystalline Si substrate realigned, and formed epitaxial columns which then grew laterally at the expense of the remaining polycrystalline grains [5]. Really the analysis of the transmission electron micrograph in Fig. 1(a) confirms this hypothesis, showing the interfacial oxide agglomerated in small beads, with average diameter of ≈2 nm. The agglomeration of the oxide film is a result of its tendency to reduce its surface energy and proceeds by surface diffusion and capillary effect [6].

If one considers the number $N$ of oxide clusters, deduced from transmission electron micrograph, per unit of lateral length, $L$, and of sample depth, $t$, passed by the electron beam during TEM observation, the superficial density of oxide molecules in the sample is

$$m = \frac{4}{3} \pi r^3 \rho \frac{N}{L}$$

(1)

Fig. 2. Cross-sectional TEM micrograph of selectively etched samples showing the emitterbase junction depth in the various cases. (a), (c) and (b) refer to samples of reference, with and without bake, respectively.
where \( r \) is the average oxide cluster radius and \( \rho \) is the number of oxide molecules per unitary volume. Assuming that the initial oxide film is uniform, we obtain the oxide thickness, \( d \)

\[
d = \frac{m}{\rho} = \frac{4}{3\pi} r^3 n,
\]

where \( n = \left(\frac{N}{L^3}\right) \).

By estimating that the sample depth, passed by the electron beam during TEM analysis, is \( \approx 10^2 \) nm, we obtain an initial surface coverage of less than 10%.

A similar morphology it is possible to observe in the sample without bake, showed in the Fig. 1(b) where the deposited Si is on the top of the figure. Also this sample shows a complete realignment of the deposited layer to the underlying silicon, and the agglomeration of the interfacial oxide layer in clusters of few nanometers. By using the Eq. (2) we estimate an initial surface coverage of less than 5%. Note that the sample was not subjected to the pre-annealing at 1025°C, for 30 s. The absence of differences in the structure of the deposited layer, in spite of the lower thermal budget, could depend on the fact that the substrate was in this case introduced into the hot deposition chamber by passing through the load-lock chamber, delaying the regrowth of additional oxide.

Conversely, no trace of any oxide cluster is detected in the sample with bake. Fig. 1(c) shows the cross-sectional TEM micrograph of this sample, in which it is possible to see an uniform contrast indicating the continuous bulk layer, and suggesting the complete removal of the oxide.

The strong difference of the interface structure does not significantly alter As diffusion into the underlying single crystal Si. The emitter-base junction depth was measured by adopting a two-dimensional delineation technique [7]. It is based on TEM observations after an appropriate sample preparation method, based on selective chemical etch of heavily doped silicon regions. The chemical solution used for this aim consisted of a mixture of nitric (65%), hydrofluoric (40%) and acetic (95%) acid, in which the dissolution of silicon is enhanced by the presence of dopant atoms. We used the HF:HNO₃:CH₃COOH solution in the ratio 1:10:10, and the selective etching was performed, for 4 s, directly on the samples already thinned to allow TEM analysis. By the comparison with a known profile, the etched regions have an As concentration of \( 3 \times 10^{18} \) cm\(^{-3} \). Therefore the boundary between the etched/non-etched Si corresponds to As concentration of about \( 3 \times 10^{18} \) cm\(^{-3} \). Fig. 2 shows the topography of the etched samples in the three investigated cases (reference, Fig. 2(a), without, Fig. 2(b) and with bake, Fig. 2(c) samples). The brighter regions of the micrographs correspond to the selectively etched As-doped Si. The figures show that the As diffused in the underlying Si substrate. In particular it reached the concentration of \( 3 \times 10^{19} \) cm\(^{-3} \) at a depth of 15 nm in the substrate of the reference sample (Fig. 2(a)), and about 5 nm in the case of the samples with and without bake (Fig. 2(b and c)). As it is possible to see in Fig. 2(a), the reference sample showed on the top of the deposited layer a number of dark particles. Note that the nominal As concentration in the as deposited sample was \( 5 \times 10^{20} \) cm\(^{-3} \), and solid solubility in As at 965°C is almost \( 2 \times 10^{20} \) cm\(^{-3} \) [8]. Therefore, the dark particles were identified as As precipitates. Samples with and without bake show, Fig. 2(b and c), not uniform contrasts on the top of the deposited layer. Diffraction analysis confirmed the crystalline array of these regions, and also the presence of twin boundaries, responsible of the different luminosity contrast on the top of the deposited layer. The TEM observations showed that the twin boundary lies along the [111] lattice planes. This [111] faceting is attributed to the growth and anisotropy in crystallization kinetics in Si, which has its slowest rate along the ⟨111⟩ direction [9]. It is note that presence of grain boundaries can strongly reduce the active fraction of dopant atom [10]. For example for a polycrystalline film, \( 5 \times 10^{20} \) cm\(^{-3} \) As doped, with grain size of 50 nm, Mandurah et al. calculated that active fraction of dopant atoms is \( \approx 0.4 \). Therefore the different diffusion of As could be due to the segregation at the grain boundary of the twins. Indeed great contribution to the different junction depths is given by the higher dopant concentration in the reference, respect to the in situ doped samples. Rutherford back scattering (RBS) analysis on the as deposited with and without bake samples showed, in fact, \( \approx 3 \times 10^{20} \) cm\(^{-3} \). As concentration, despite of the reference sample, with \( 5 \times 10^{20} \).
As doped. We can conclude that strong differences in the polycrystalline/single crystal Si interface do not play any evident role in the As diffusion process.

Conversely this interface strongly influences the Gummel plot of these devices, i.e. collector and base currents as a function of the base-emitter voltage. We measured those currents for a number of devices of each type. Fig. 3 shows the typical results. Note that transistor without bake does not show particular differences respect to the reference device, despite of the different mechanisms of doping and the different SiO$_2$ clusters concentration. This suggests that the in situ doping process does not change the electrical characteristics of the device. Only the transistor with bake shows significant differences compared to the other devices, and in particular it exhibits a higher base current. That suggests that it is the Si/polysilicon interface, rather the polysilicon doping mechanism, which plays the major role in determining device electrical characteristics. Indeed, the collector current $I_C$ is mainly determined by the flow of electrons through the emitter to the base and collector. Considerable evidence has shown that the potential barrier to electrons, associated to the interfacial oxide, is small, and the tunneling probability is high. That produces only a little reduction in the electron flow. Conversely, the base current $I_B$ is determined mainly by the flow of holes from the base into the emitter. The potential barrier to holes associated to the oxide layer is high, the tunneling probability is low, and so the hole flow is significantly reduced. The current gain is the ratio $I_C/I_B$ and so the gain is increased [10].

![Fig. 4. Base resistance from Sparameters measurements as a function of frequency, in the active region at $V_{BE}=0.9$ V and $V_{BC}=1$ V, in the reference transistor ( ), with (---) and without bake (---).](image)

![Fig. 5. Output characteristics for the reference device (a), and for the transistors with (b) and without bake (b).](image)

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not bias the intrinsic base, and only the extrinsic base contributes to the effective base resistance. Note that at any frequency, in the case of the transistor with bake we find a considerably lower parasitic base resistance, indicating that the contribution of the intrinsic base resistance is negligible. This result suggests that the Boron doping level in the intrinsic base in the case of the device with bake is higher than the doping levels in the other devices. The base resistance was also measured by using a direct dc measurements in transistors with two base contacts. The obtained results confirmed the base resistance trends of Fig.4.

The higher Boron concentration present in transistor with bake is confirmed by the output characteristics, obtained by monitoring the collector current as a function of the collector emitter voltage, at different fixed base currents. The results of these measures are reported in Fig. 5. Fig. 5(a) shows that, in the reference device, collector current I_C rapidly increases at V_CE of about 2 V, because of the punch-through effect [11]. Device without bake (Fig. 5b) shows the collector current increase at V_CE of about 2.5 V. On the contrary in the device with bake the punch-through is observed only when V_CE = 3 V, i.e. breakdown voltage in with bake device is higher respect to the other ones. The result is correlated to higher Boron concentration in the region close to the junction in device with bake. It can be related to the absence of the interface oxide, observed in this case. In fact, the SiO₂ interface clustering found in the devices of reference and without bake may give raise to an enhancement of B diffusion similar to oxidation enhanced diffusion which decreases, compared with the case with bake, the residual B dose in the base. Finally, we note that in the three cases, the devices maintain remarkable high frequency characteristics, as shown by the data of cut-off frequency as a function of collector current reported in Fig. 6.

4. Conclusions

In this paper we have reported structural and electrical characterization of three kinds of emitter bipolar transistors. These devices were fabricated with identical standard processing, except for the different treatments of the interface between the polycrystalline Si and the underlying single crystal Si in the emitter region, and different emitter doping mechanisms. We demonstrated that by doping in situ the emitter polysilicon layer, the Gummel plot of the device do not show any difference respect to the device with emitter doped by standard ion implantation, suggesting that a different doping mechanism does not influence the As diffusion. In one of the investigated types of devices, the interface in the emitter region was in situ cleaned before the emitter polysilicon deposition, thus giving an oxide free interface. In that case the electrical characteristics of the transistors, showed significant differences respect to device with interfacial thin oxide. As expected, in fact, base current was one order higher in respect to the other transistors. We have shown that, in the same device, the base resistance was one order lower in respect to the other two kinds of devices. It suggested a higher Boron concentration in the intrinsic base region of the interfacial oxide free transistor, in spite of the identical doping and heat treatments performed. The presence of the high Boron concentration, close to the junction, was also confirmed by the output characteristics, showing that breakdown voltage was higher in respect to the other transistors.

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References