Defect generation in ultrathin silicon dioxide films produced by anode hole injection

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A direct demonstration of defect generation in ultrathin silicon dioxide films due to the transport of holes through this layer is reported. These defects are observed only when the hole current to the cathode of the device exceeds the electron current to the anode. This condition is produced on p-channel field-effect transistors under negative gate-voltage-bias conditions with ultrathin gate oxide layers. These results are related to current reliability models which use anode hole injection and the defects produced to explain destructive breakdown of the oxide layer. © 2000 American Institute of Physics.

Models with anode-hole injection (AHI) have been used for the past 15 years to explain the “intrinsic” breakdown of the silicon dioxide (SiO₂) layers used in the gates of capacitors and field-effect transistors (FETs). In most of these models, electrons (injected from the cathode and heated by the applied electric field while traversing the oxide layer) enter the anode of the device where they can generate hot holes by majority or minority carrier ionization. These hot holes are then injected over or through the anode/oxide interface energy barrier and traverse the oxide layer to the cathode, producing point defects (i.e., traps and interface states) along the way. The production of these defect sites eventually causes destructive breakdown of the gate oxide and device failure. Although these models are physically elegant, there has been a lack of direct experimental evidence demonstrating that hole transport occurs and produces these oxide defects. The main supporting experimental evidence has come from carrier separation measurements on n-channel FETs (n-FETs) with gate oxide thickness in the range from 4 to 10 nm under inversion conditions at positive gate voltage ($V'_g$). In these studies, a small hole current observed in the silicon substrate of the FET was attributed to holes coming from the anode gate electrode. However, recently this small hole current has been shown to have components from both the creation of generation-recombination centers in the silicon (Si) substrate and light coming from the gate with energies greater than the silicon band gap (about 1 eV) which could obscure any anode hole current. Because of energy barrier asymmetries between electrons and holes, nonenergetic hole injection by tunneling is difficult without simultaneous electron injection, except for the situation which will be discussed here. This case (depicted in Fig. 1) occurs only on p-channel FETs with ultrathin oxides under inversion operating conditions. Using these devices, direct measurements of holes flowing from anode to cathode will be correlated to oxide defect generation.

The devices used in this study were fully processed n- and p-channel FETs with n-degenerate ($n^+$) and p-degenerate ($p^+$) polycrystalline silicon (poly-Si) gates, respectively, fabricated using a complementary metal–oxide–semiconductor base technology. Gate areas were equivalent to or less than $2 \times 10^{-6} \text{ cm}^2$ to minimize series resistance effects. Gate oxide thickness was in the range from 1.4 to 2.5 nm, thermally grown in either N₂O (about 1% N), NO or N implantation of Si followed by N₂O (about 8% N). The results reported here did not depend significantly on differences in gate oxide processing or nitrogen content of the oxide. The degradation probabilities (defect sites generated per injected carrier) were determined using the stress-induced-leakage-current (SILC) sensing techniques for bulk electron traps generated after stressing the device at constant

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**FIG. 1.** Carrier separation measurements on ultrathin gate oxide (1.6-nm-thick, N₂O grown) p-FET/p⁺ structure under inversion conditions ($V'_g$) showing the magnitude of the gate, p-channel, and n-well currents as a function of the gate voltage. Inset shows corresponding energy band diagram.

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**References**

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gate voltage for increasingly larger amounts of total injected carrier fluence ($Q_{inj}$). Only electron SILC sensing was used under $V_g^+$ conditions. All sensing measurements were performed immediately (within seconds) after stress to minimize effects due to slow charging/discharging of the as-fabricated or generated sites. Since SILC measurements only give a relative measure of defect generation, device characteristics (i.e., drain current versus gate voltage biased in the linear regime) were used to determine the absolute number of interface states (from subthreshold slope) and interface charges (from threshold voltage shift) which were simultaneously generated. Also, carrier separation measurements were performed to determine the appropriate carriers (electrons or holes) flowing through the gate oxide under the stressing (or sensing) conditions used. In these measurements, separate determination of the carriers contributing to the total gate current are made by also measuring the channel and substrate currents of the FET. Device stressing was performed using either direct tunneling of thermal carriers under constant voltage-bias conditions, or substrate-hot-hole (SHH) injection. This latter mode of stress could be used on the same devices to generate a hot-hole distribution at the injecting $p$-channel anode/oxide interface by forward biasing the $p$-Si substrate relative to the $n$ well containing the $p$-FET. The average energy of these hot holes could be varied using the voltage bias applied to the $n$ well ($V_{well}^+$) and/or the gate electrode ($V_g^+$). However, these gate voltage magnitudes were kept below 1 V to minimize simultaneous electron injection from the Si valence band of the poly-Si gate electrode (see Fig. 1). All stressing and sensing measurements were performed at room temperature.

Figure 1 shows carrier separation data for a $p$-FET with a 1.6-nm-thick gate oxide under inversion operating conditions (i.e., for $V_g^+$). Here, holes tunneling from the inversion layer (near the top of the Si valence band) through an $\approx 5$ eV energy barrier to filled valence band states in the gate of the device dominate the total gate current to about $-2.5$ V. The electron current simultaneously measured on the $n$ well of the $p$-FET is not observed until gate voltages exceeding $-1$ V and begins to dominate the gate current at voltages above $-2.5$ V. This electron current is due to valence band tunneling from the $p^+$ poly-Si gate through an $\approx 4$ eV energy barrier to empty conduction band states in the $Si$ substrate. This also accounts for the suppression of this current to $-1$ V from the unavailability of empty states across the silicon band gap of the substrate for these tunneling electrons (see inset in Fig. 1). This interpretation of the electron current observed in the $p$-FET is confirmed by the equivalence of this data to that for the the hole substrate current measured during carrier separation on the $n$-FET shown in Fig. 2. This current is due to the holes left behind by electron valence band tunneling to empty conduction band states in the $n^+$ poly-Si gate electrode under $V_g^-$. The $n$-FET carrier separation data in Fig. 2 also show that the gate current for this device is always dominated by electrons tunneling from the inversion layer (near the bottom of the Si conduction band) to empty conduction band states in the gate. For accumulation conditions on the $p$-FET under $V_g^+$ or on $n$-FET under $V_g^-$, the gate current is dominated by the larger electron currents from the Si conduction bands. This is due to differences in the energy barrier heights for the tunneling carriers ($\approx 3$ eV for electrons and $\approx 5$ eV for holes). Increasing the gate oxide thickness reduces all tunneling currents with hole current dominance for the $p$-FET under inversion conditions moving to smaller negative gate voltages.

Figure 3 shows data for the SILC generation probability ($P_{gen}$) as a function of the gate voltage under inversion conditions on similar $p$-FETs and $n$-FETs. The stress conditions used here produced a source of thermal carriers near the appropriate injecting interface. The SILC generation probability is determined from the slope of the normalized gate current increase (near a ratio of 0.01) as a function of the total injected carrier fluence in a regime that is considered

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linear after correction for background charging effects. The normalized SILC increase is defined as $\Delta J / J_0$, where $\Delta J = J - J_0$ with $J_0$ and $J$ being the initial gate current of the as-fabricated device and the gate current after voltage stress, respectively. Data for $P_{\text{gen}}$ under the accumulation mode of operation for the $p$-FETs and $n$-FETs (not shown) yielded similar values to those shown for the $n$-FET under inversion conditions (i.e., for $V_g^+$), consistent with SILC measurements on thicker gate oxide devices. Measurements of the absolute number of generated interface charges (positive for $p$-FETs and negative for $n$-FETs) determined from FET characteristics of devices with low-nitrogen-concentration gate oxides (N$_2$O grown) yielded the same behavior as shown in Fig. 3 with a proportionality constant (compared to SILC measurements of bulk electron traps) similar to previous reports. However, for the $p$-FETs with high-nitrogen-concentration gate oxides (NO grown) an additional positive charge component was observed under inversion stressing conditions, consistent with recent observations by other investigators.

In Fig. 3 $P_{\text{gen}}$ values for $p$-FET and $n$-FET inversion showed a similar dependence on the magnitude of the gate voltage down to about 3 V independent of gate oxide processing. However, below this 3 V magnitude, $P_{\text{gen}}$ for the $p$-FET is larger than corresponding values for the $n$-FET, but has a weaker gate voltage dependence. This coincides with hole injection from the $p$-FET channel dominating the gate current as shown in Fig. 1. In Fig. 4, $P_{\text{gen}}$ for defects created under inversion conditions by direct tunneling of either thermal (from Fig. 3) or hot holes (generated using SHH injection) are compared as a function of the maximum energy ($E_{\text{max}}$) delivered to the holes to the $p^+$ poly-Si gate. For thermal and hot holes, the $E_{\text{max}}$ values are assumed to be equivalent to $qV_g^-$ and $qV_g^+ + |q|(V_{\text{well}} + \phi_{p/n})$, respectively, where $q$ is the charge on electron ($\sim 1.6 \times 10^{-19}$ C) and $\phi_{p/n}$ is the contact potential difference of 1.1 V between the $p^+$ inversion layer and the $n^+$ contact to the $n$ well. This assumption for SHH stress is reasonable given the short depletion width in the heavily doped $n$ well ($\sim 1 \times 10^{18}$ cm$^{-3}$) and selective filtering of the hottest carriers by the tunneling process. For SHH stress, both constant gate (+ symbol) or constant well ($\bigcirc$ symbol) voltage bias conditions were used. This comparison in Fig. 4 shows that $P_{\text{gen}}$ depends only on the total electron energy delivered by the tunneling holes to the poly-Si gate and not on the initial energy distribution at the anode $p$-channel/oxide interface.

The studies presented here show that holes injected from the anode can produce bulk oxide defects. However compared to electrons, a weaker energy dependence is observed. When both carriers are flowing through the oxide layer, the hole current must be at least comparable to the electron current to observe any additional contribution to total defect buildup. These observations imply that defect generation models using a small anode hole current relative to the larger electron current are problematical for explaining defect creation, particularly for $n$-FETs under inversion conditions. Future studies will correlate destructive breakdown of the ultrathin gate oxides with the defect generation probability for $p$-FETs under low-voltage inversion conditions where defect buildup is determined primarily by tunneling holes.

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