A 90 nm Communication Technology Featuring SiGe HBT Transistors, RF CMOS, Precision R-L-C RF Elements and 1 $\mu$m$^2$ 6-T SRAM Cell


Logic Technology Development

Intel Corporation, Hillsboro, OR 97124, USA
Outline

- Technology Features
- CMOS
- SiGe:C HBT
- Isolation
- Passives
- Validation Vehicles
- Conclusions
Integration

Baseline CMOS

- Shallow Trench Isolation
- CMOS Well Implants
- Thin gate and poly
- Tip implants
- Spacer Formation
- NSD/PSD
- Silicide & contacts
- Metal 1-6 Layers
- Metal 7

Communications

- High resistivity substrate
- Triple Well (deep n-well)
- LP CMOS 15Å (1.2V)
- Analog CMOS 50Å (2.5V)
- SiGe HBT module
- Poly Resistor
- MIM Capacitor / TF resistor
- Inductors
### Matching Circuit Needs to Device Type

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Logic and analog MOS are the foundation for the majority of critical communications circuits.
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**Precision single elements are key to many circuits**
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Most circuits have multiple implementation paths, redundancy is important in process definition.
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Specialized BJT devices cover gaps where MOS falls short
90nm CMOS
Performance versus Low Power

Performance Devices
Low Power Devices

CV/I (Gate delay in pS)

I_{OFF} (nA/μm)

10000
1000
100
10
1
0.1
0.01

0.5 1.5 2.5 3.5
90nm Communications CMOS
RF Performance (Low Power Device)

NMOS: 225/143 $F_T/F_{\text{MAX}}$
PMOS: 114/70 $F_T/F_{\text{MAX}}$

(Vg=0.7V, Vds=1.2V)
This work

\[ F_T: \text{Intrinsic NMOS Performance} \]

![Plot showing intrinsic NMOS performance with labeled references.](image-url)

- This work
- Reference [1]
- Reference [2]
- Reference [3]
- Reference [4]
- Reference [6]
$F_T$: Intrinsic PMOS Performance

$F_T$ (GHz)

(CUT-OFF FREQUENCY)

$L_{GATE}$ (μm)

This work

[6]

[7]

[8]
Fmax: Layout

- **Make $R_G$ small**
  - Two-sided gates
  - Minimize field extension
  - Contacts close to devices
  - Multiple fingers

- **Minimize pad coupling**
  - HiRES substrates
  - Isolate/shield signal pads
  - Use higher-level metal

- **Minimize cap/scatter**
  - Isolate gate from drain
  - Taper source bus

Comparison of CMOS: $F_T$ and $F_{MAX}$

This work

$F_{MAX}$ (MAX OSC. FREQUENCY)

$F_T$ (GHz) (CUT-OFF FREQUENCY)

Outline

- Technology Features
- CMOS
- SiGe:C HBT
Criteria for BJT device definition

- Manufacturing simplicity
- Maximum leverage of the main 90nm microprocessor process (all tools shared, no special tools)
- Meets the needs of the circuit design community
- No impact to CMOS performance
SiGe:C HBT Architecture

Quasi-self-aligned chosen as the better tradeoff between manufacturing complexity and performance.
HBT: SiGe:C Epitaxy


Baseline: 130/100 $F_T/F_{MAX}$

-20dB/dec

FREQUENCY (GHz)

Cum Prob %

300 mm BASELINE LOT, WIW and WTW $F_T$ VARIATION (GHz)
No CMOS Degradation

- NMOS and PMOS $I_{ON}$ versus $I_{OFF}$ characteristics are not degraded by HBT integration
BJT Yield issues: impact of volume

Incoming to EPI

Increased wafer volume generated
Ge deposits on chamber walls:
Fixed with purges and pre-coats

OLD Process
Start of epi dep

OLD Process
After epi dep

NEW Process
Start of epi dep

NEW Process
After epi dep

IEDM 2002
Outline

- Technology Features
- CMOS
- SiGe:C HBT
- Isolation
Isolation: P- versus P+ epi (with DNW)

Guard ring on p+ epi (LoRes)
Guard ring on p- (HiRes)
DNW on P- (HiRes)
DNW on P+ epi (LowRes)

S21 (dB)

10 MHz 100 MHz 1 GHz 10 GHz 100 GHz
10 MHz 100 MHz 1 GHz 10 GHz 100 GHz

S21 = forward transmission gain/loss
Substrates: Latch-up, P- versus P+ epi

Merrill, R.B.; Young, W.M.; Brehmer, K. Effect of substrate material on crosstalk in mixed analog/digital integrated circuits.

Substrates: Latch-up, P- versus P+ epi with and without DNW

HOLDING VOLTAGE (V)

P- (50 ohm-cm)

DNW (magenta)
No DNW (cyan)

N+ TO PWELL TAP DISTANCE (microns)
Outline

- Technology Features
- CMOS
- SiGe:C HBT
- Isolation
- Passives
MIM Capacitor BiasTemp. Reliability (T=125C)

TTF seconds
(0.2% C at Bias=0V, 1MHz)

Bias (V)

0 5 10 15 20 25 30

1.E+01
1.E+03
1.E+05
1.E+07
1.E+09

MIM Cap CV >

< MIM Cap Bias Temp.

317 years
MIM Capacitor Reliability

OLD Process

New Process

MIM CAP LEAKAGE AT HIGH BIAS [A]

Before Stress

After Stress

A=5.2k um²
A=26k um²
A=130k um²

Cum Prob %

99.9%
99%
90%
80%
70%
60%
50%
40%
30%
20%
10%
1%
0.1%

1.0E-07 1.0E-06 1.0E-05 1.0E-04

Qbd (C/cm²)

Cum %
Hi-Q Inductor Library Templates

Focusing on lower L, Hi-Q inductors to support 10/40G circuits
Hi-Q Inductor Library Templates

This work
Measuring Q

\[ Q = \frac{-\text{Im} \ (Y_{11})}{\text{Re} \ (Y_{11})} \]

FREQUENCY
(250.0MHz to 50.25GHz)
Measured versus simulated Q

Inductor Dimension:
Do = 154 um  W = 12 um
S = 1 um  T = 1.5

Simulated
Measured

FREQUENCY
1GHz  10 GHz

Q
-10  0  10  20
Hi-Q Inductors and substrates

![Graph showing PEAK Q vs FREQUENCY (GHz) for different materials and conditions.]

- 50 ohm-cm w/o parasitic control
- P+ epi w/o parasitic control
- 50 ohm-cm with parasitic control
- P+ epi with parasitic control
Validation vehicles

A large variety of learning vehicles are being supported. Illustrated is an LC-VCO from a 10G SerDes test circuit.
Intel CMOS 10G SerDes Test Circuit
Transmit PLL – Measured Jitter

Meets jitter transfer function specification >

OC-192 Specification is integral under curve = 100 mUI;
Actual performance is 40 mUI ~ 2X better
Conclusions

- Manufacturable communications process integrated into 90nm digital CMOS
- RF NMOS devices at $225/140 \frac{F_T}{F_{MAX}}$
- RF PMOS devices at $114/70 \frac{F_T}{F_{MAX}}$
- Baseline HBT device at $130/100 \frac{F_T}{F_{MAX}}$
- Reliable $1.15 \frac{fF}{\mu m^2}$ Cu-MIM and resistor
- Hi-Q inductors
Acknowledgment

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– PTD Process and Design Groups
– Sort Test Technology Development
– Quality and Reliability Engineering
– Technology Computer Aided Design
References


References


A soft copy of this and other recent Intel presentations can be found at:

www.intel.com/research/silicon