

# Chapter 4

# Wafer Manufacturing and Epitaxy Growing

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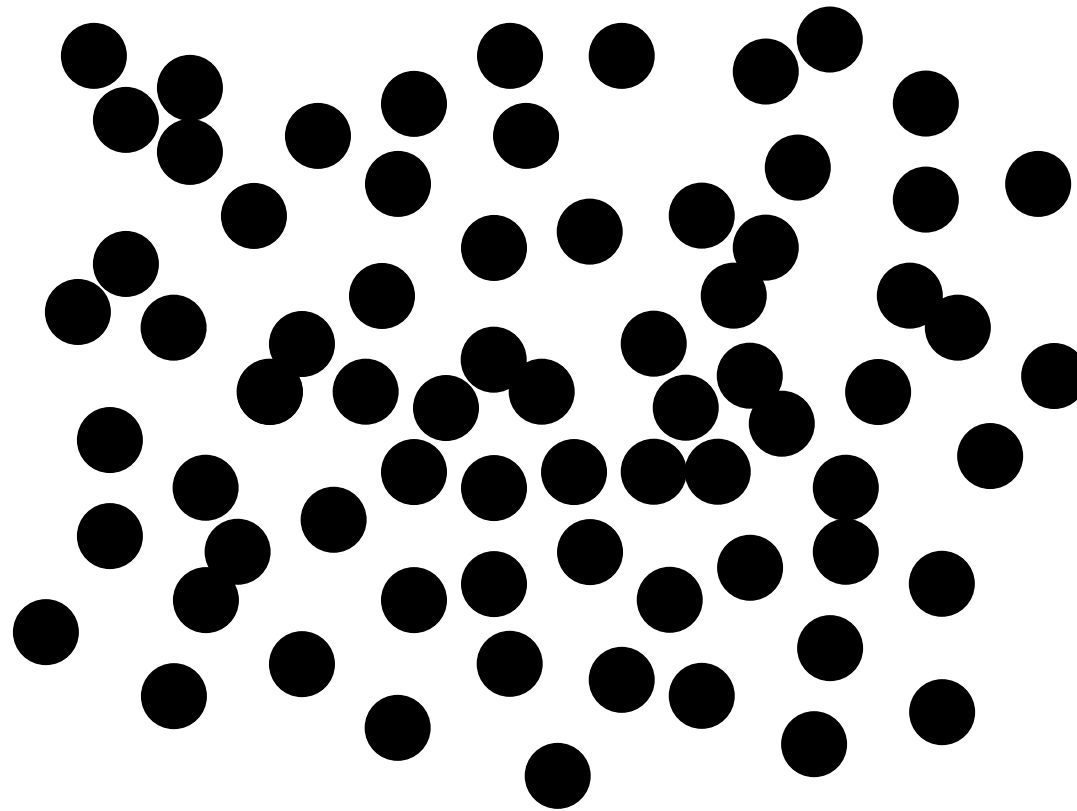
# Objectives

- Give two reasons why silicon dominate
- List at least two wafer orientations
- List the basic steps from sand to wafer
- Describe the CZ and FZ methods
- Explain the purpose of epitaxial silicon
- Describe the epi-silicon deposition process.

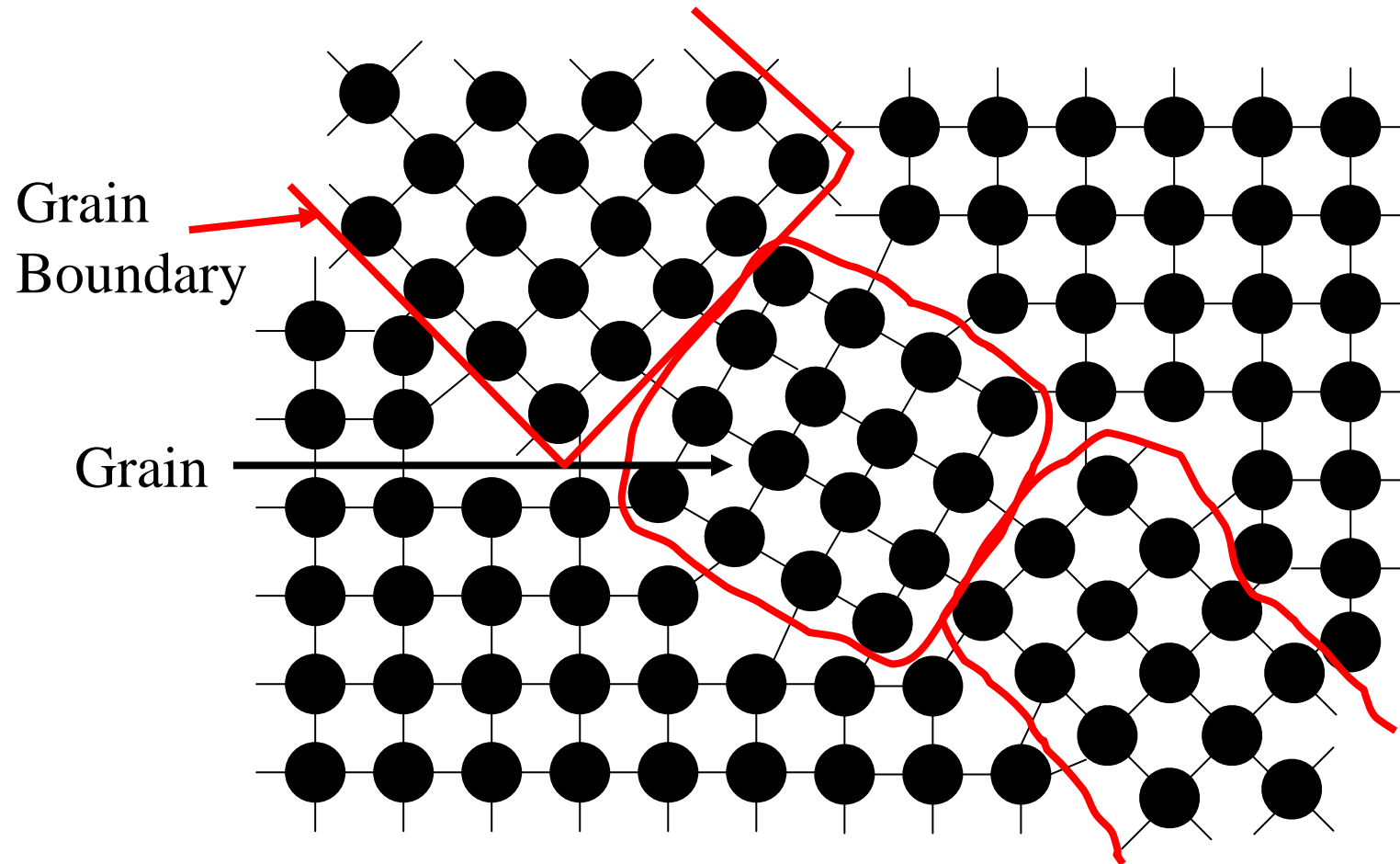
# Crystal Structures

- Amorphous
  - No repeated structure at all
- Polycrystalline
  - Some repeated structures
- Single crystal
  - One repeated structure

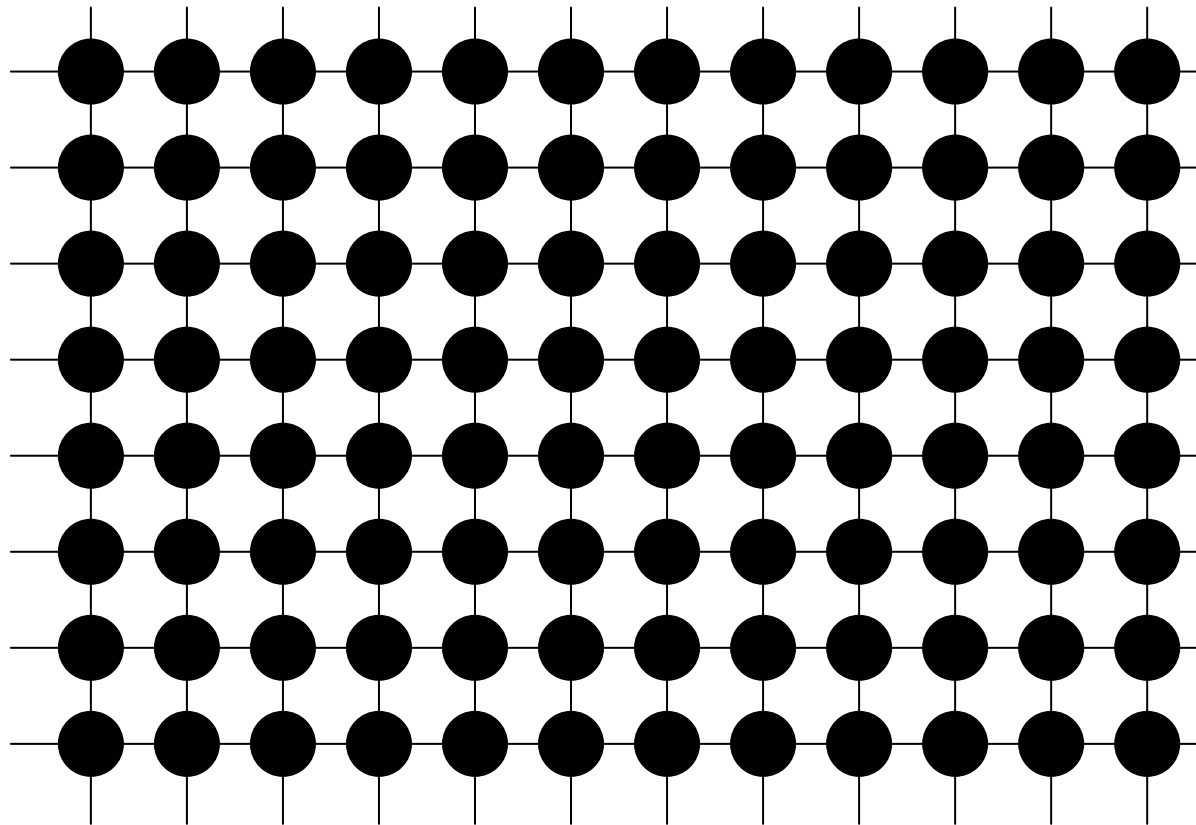
# Amorphous Structure



# Polycrystalline Structure



# Single Crystal Structure



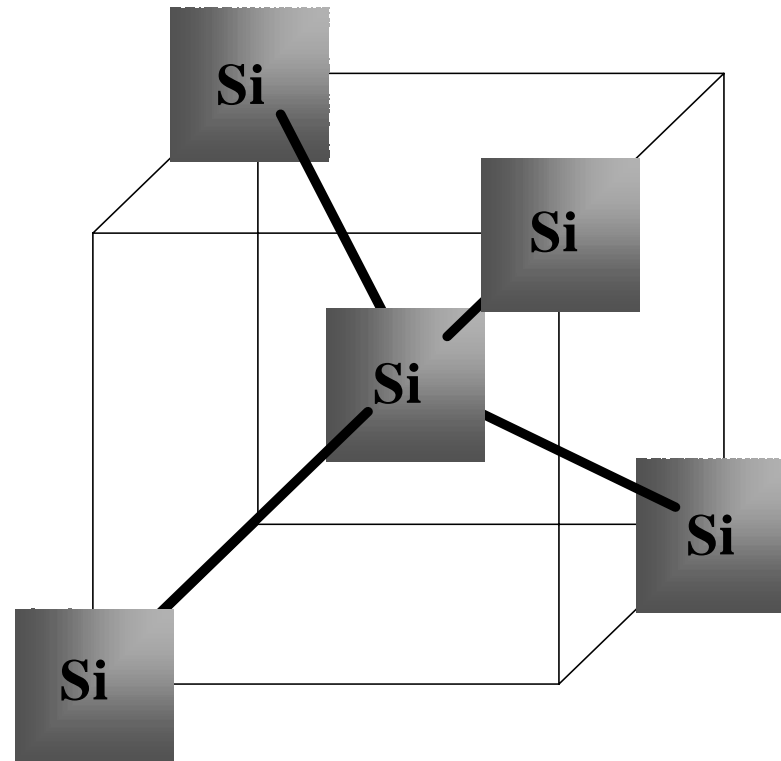
# Why Silicon?

- Abundant, cheap
- Silicon dioxide is very stable, strong dielectric, and it is easy to grow in thermal process.
- Large band gap, wide operation temperature range.

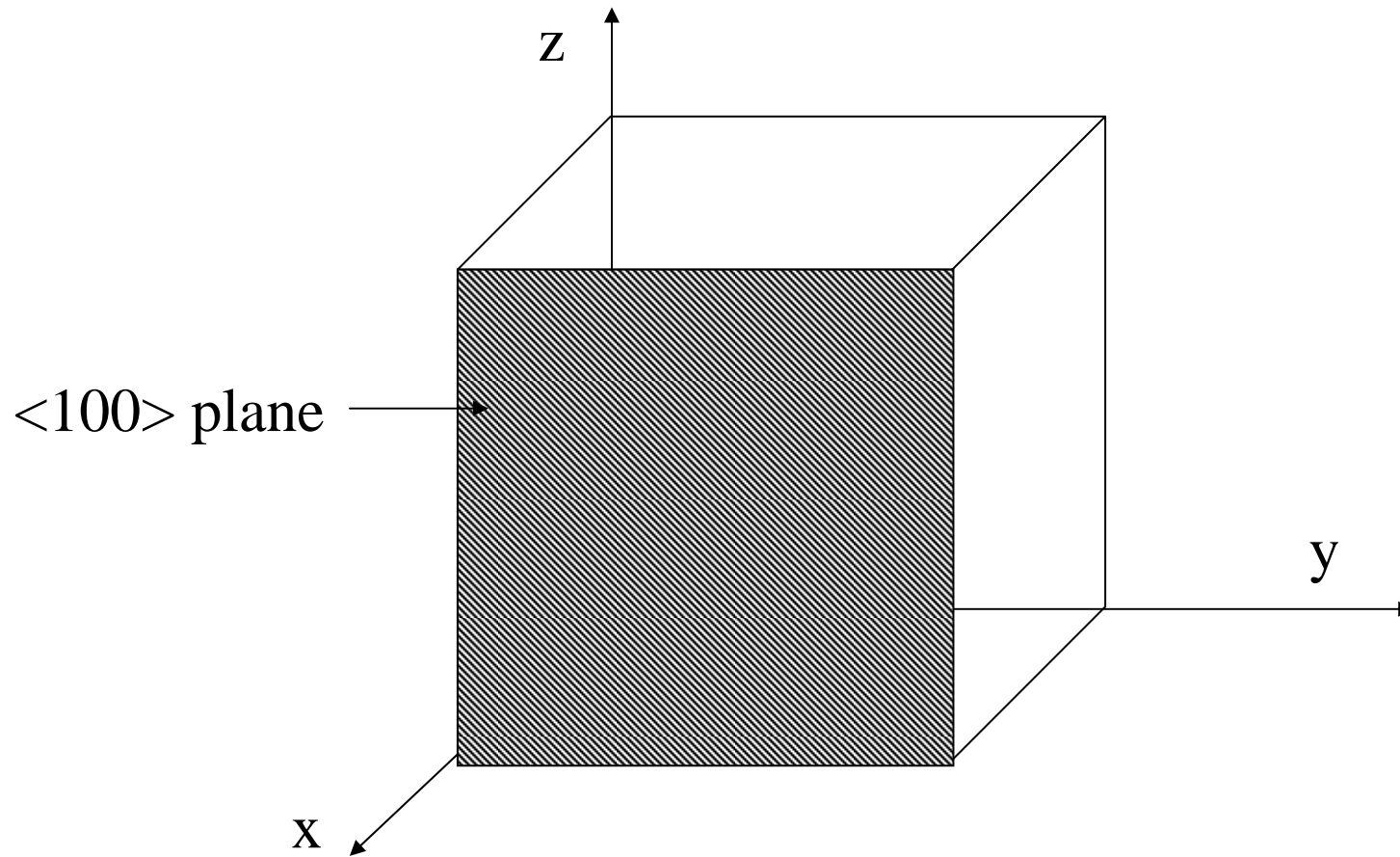
Name	Silicon
Symbal	Si
Atomic number	14
Atomic weight	28.0855
Discoverer	Jöns Jacob Berzelius
Discovered at	Sweden
Discovery date	1824
Origin of name	From the Latin word "silicis" meaning "flint"
Bond length in single crystal Si	2.352 Å
Density of solid	2.33 g/cm <sup>3</sup>
Molar volume	12.06 cm <sup>3</sup>
Velocity of sound	2200 m/sec
Electrical resistivity	100,000 μΩ·cm
Reflectivity	28%
Melting point	1414 °C
Boiling point	2900 °C



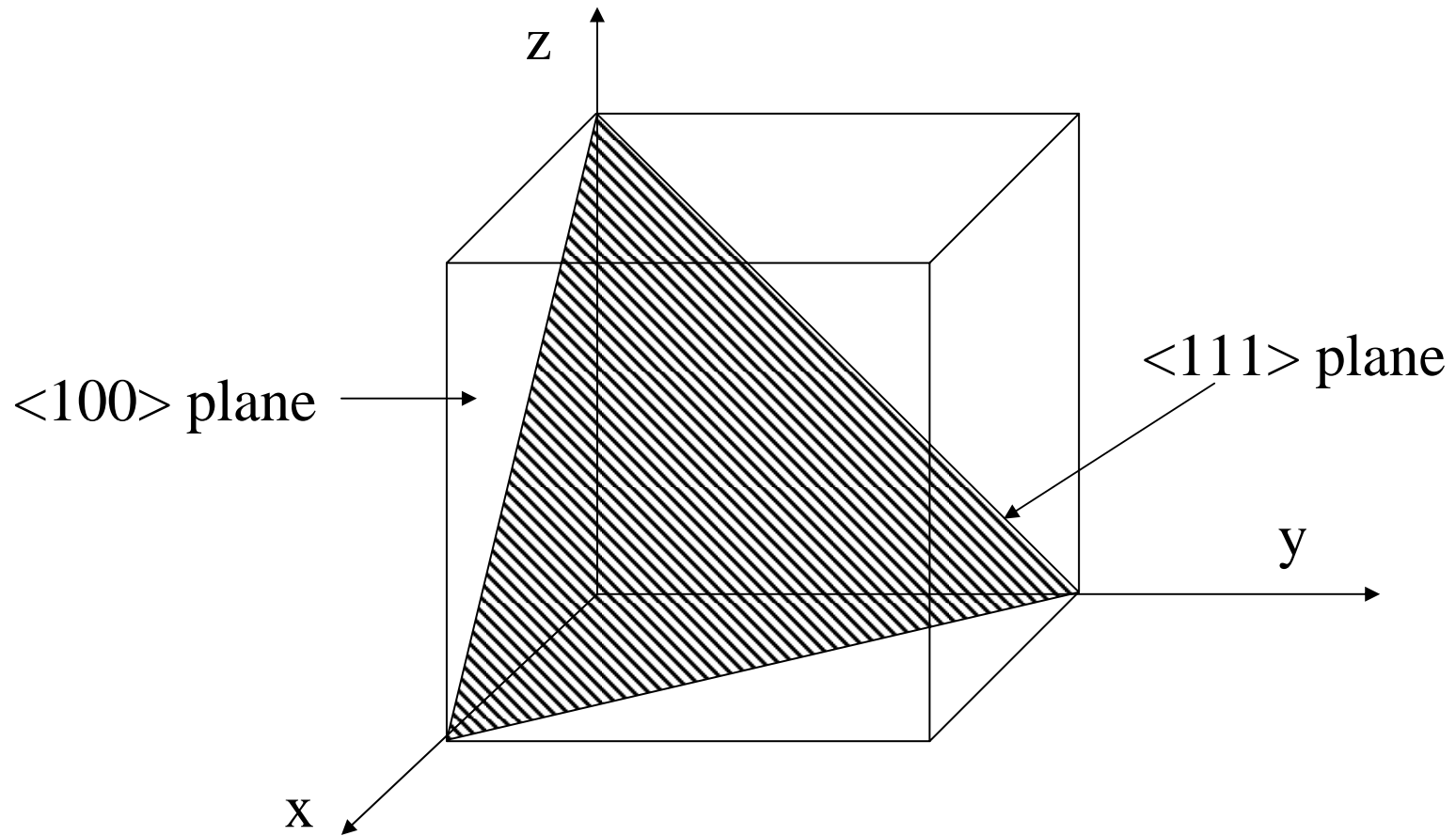
# Unit Cell of Single Crystal Silicon



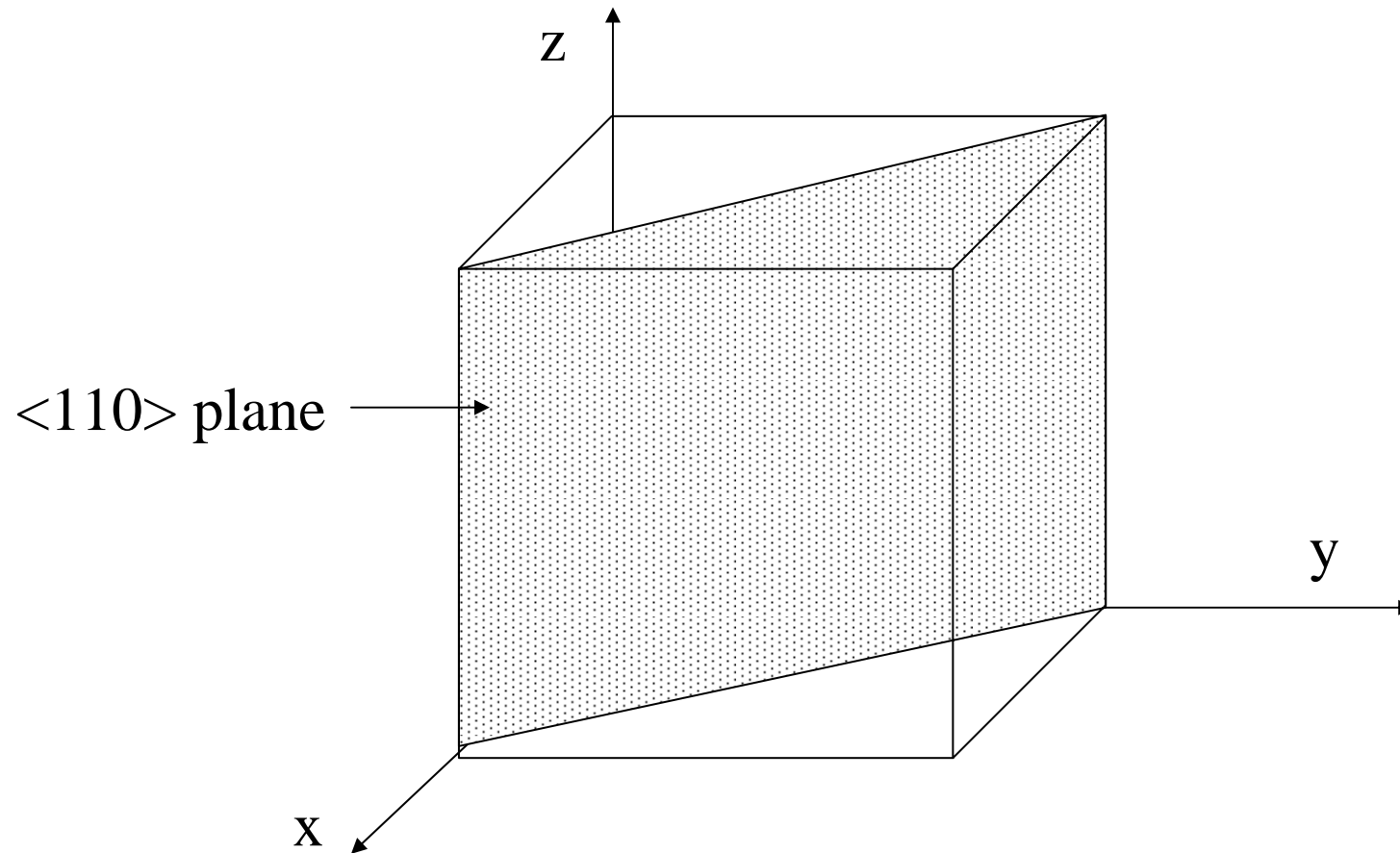
# Crystal Orientations: $\langle 100 \rangle$



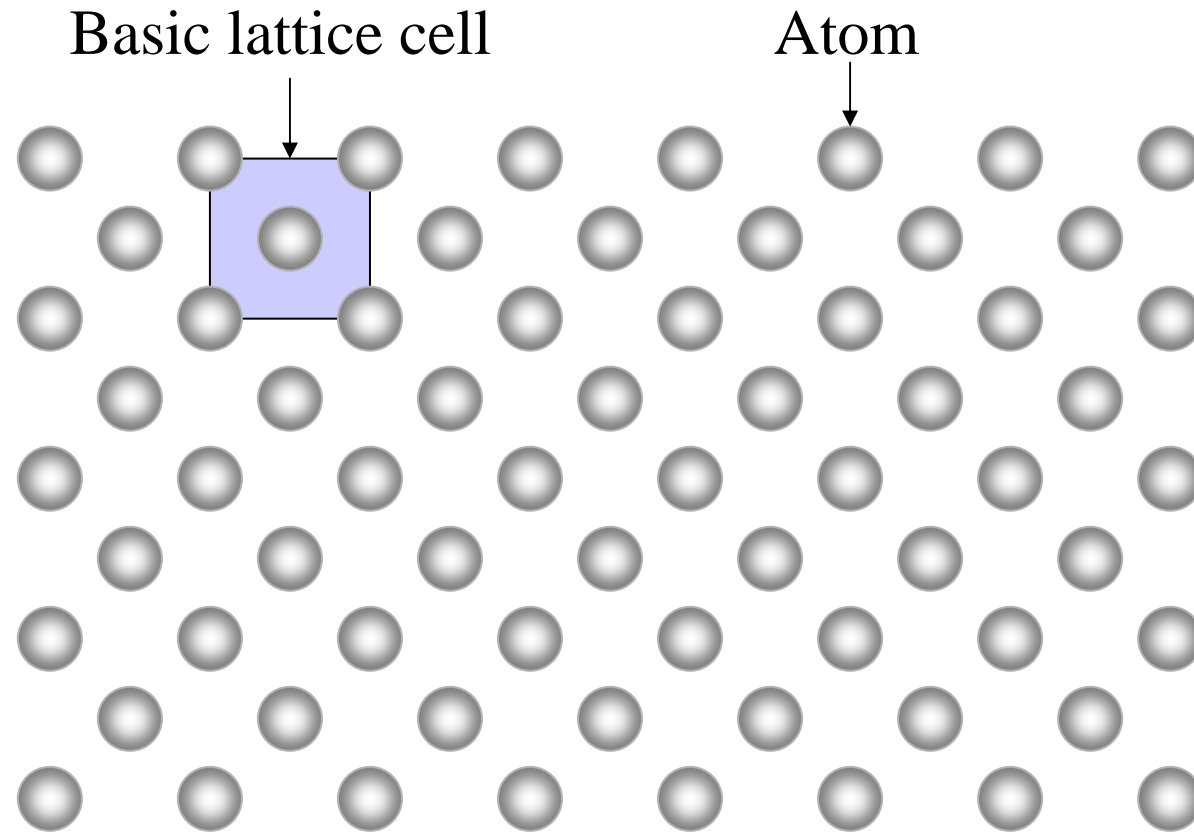
# Crystal Orientations: $\langle 111 \rangle$



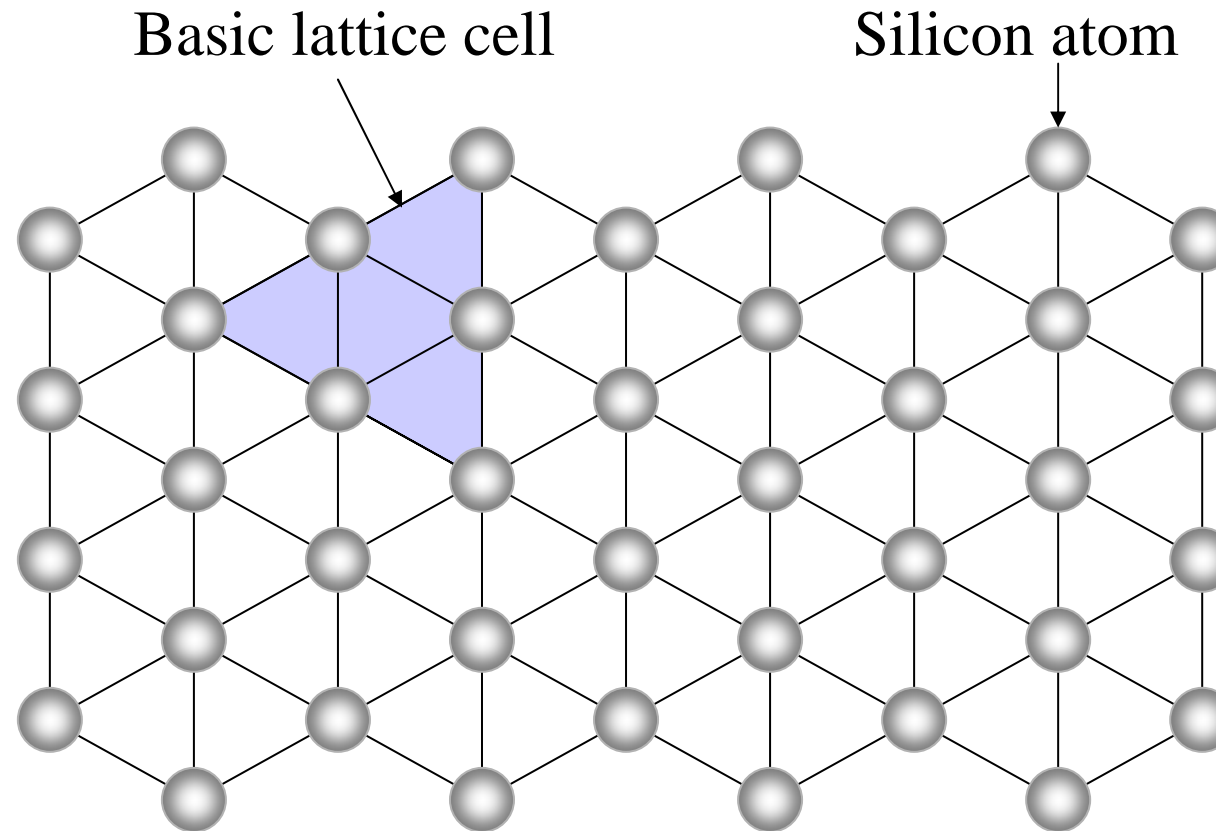
# Crystal Orientations: $\langle 110 \rangle$



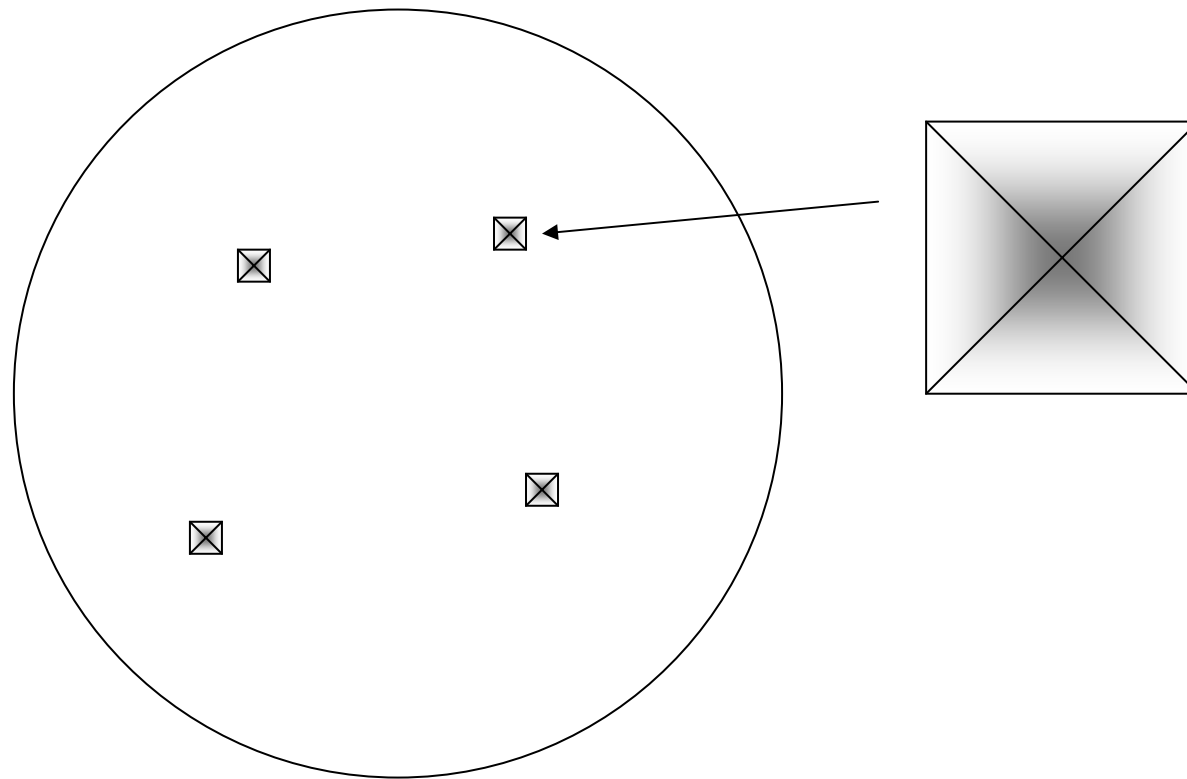
# $\langle 100 \rangle$ Orientation Plane



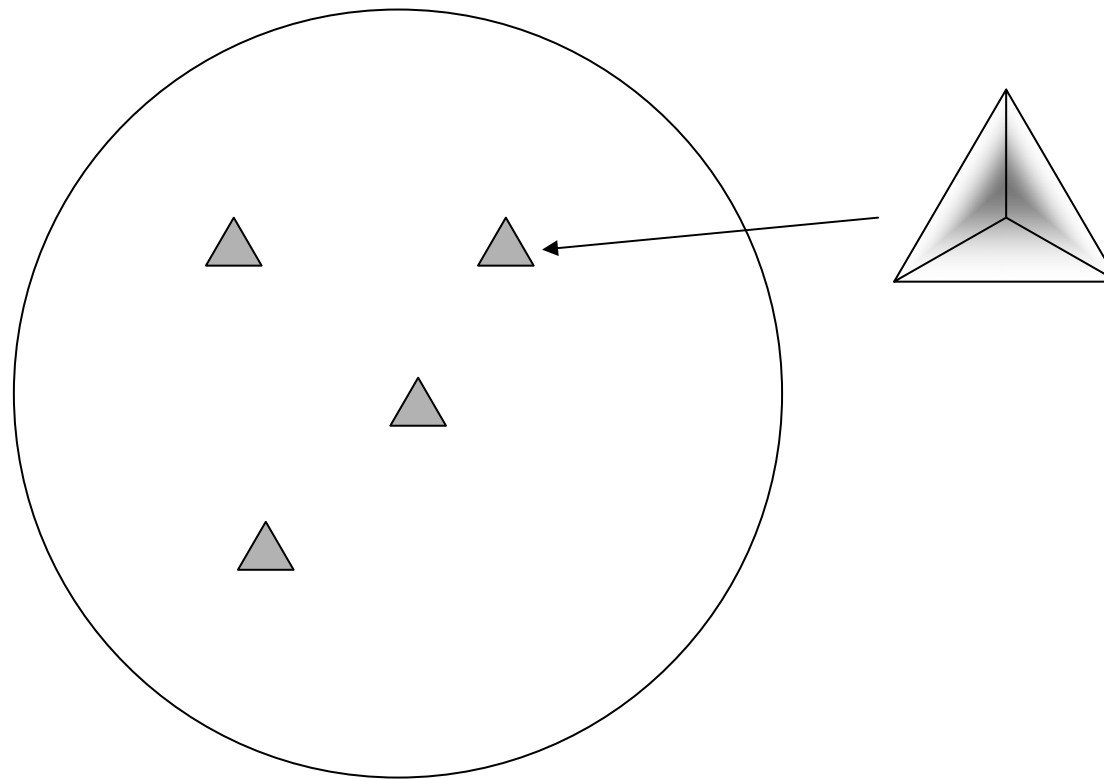
# $\langle 111 \rangle$ Orientation Plane



# $\langle 100 \rangle$ Wafer Etch Pits

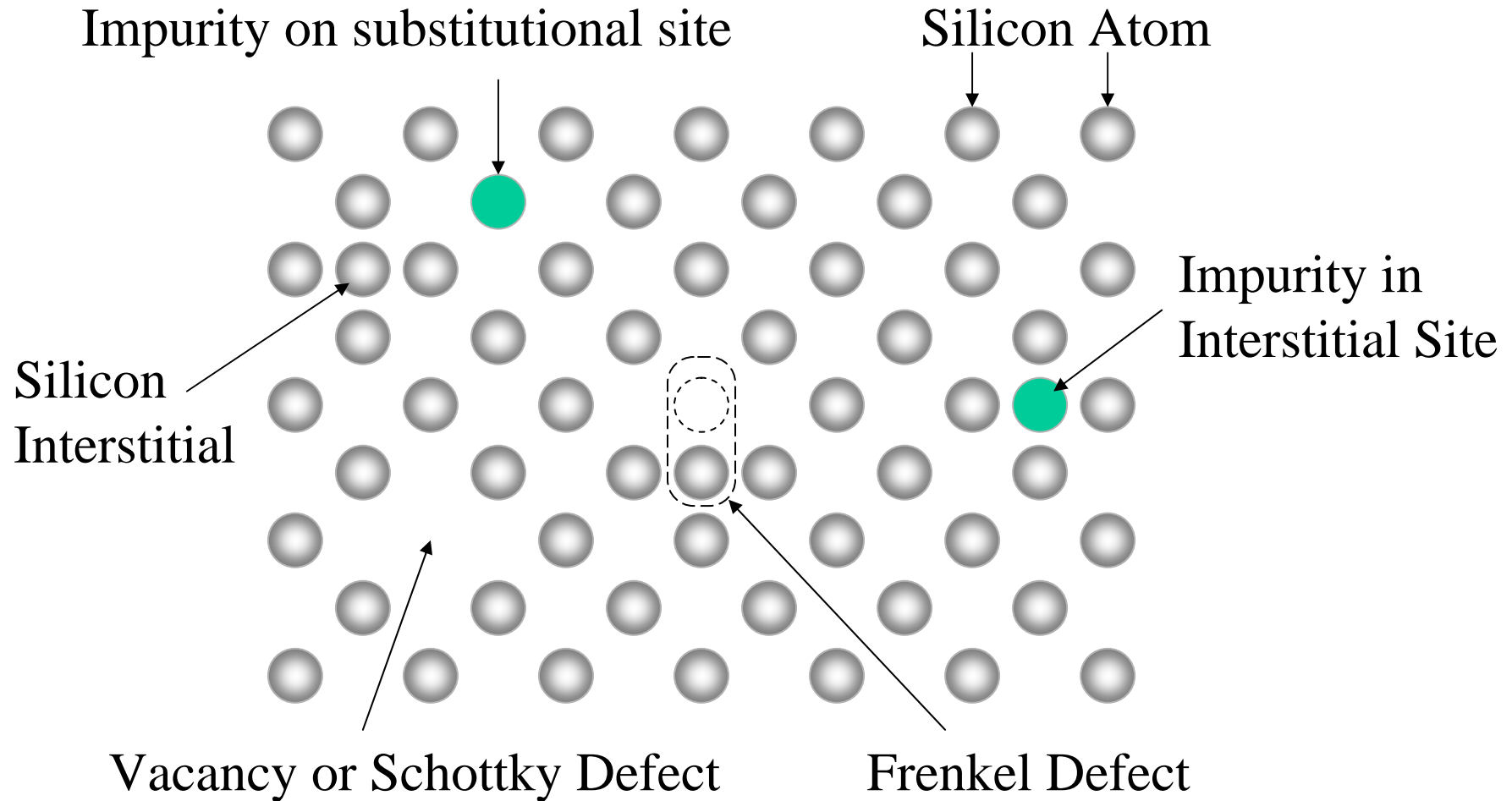


# $\langle 111 \rangle$ Wafer Etch Pits

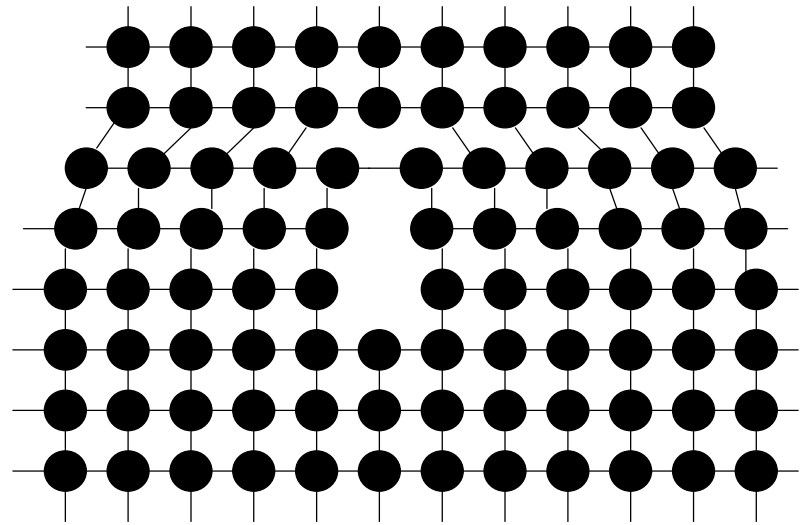
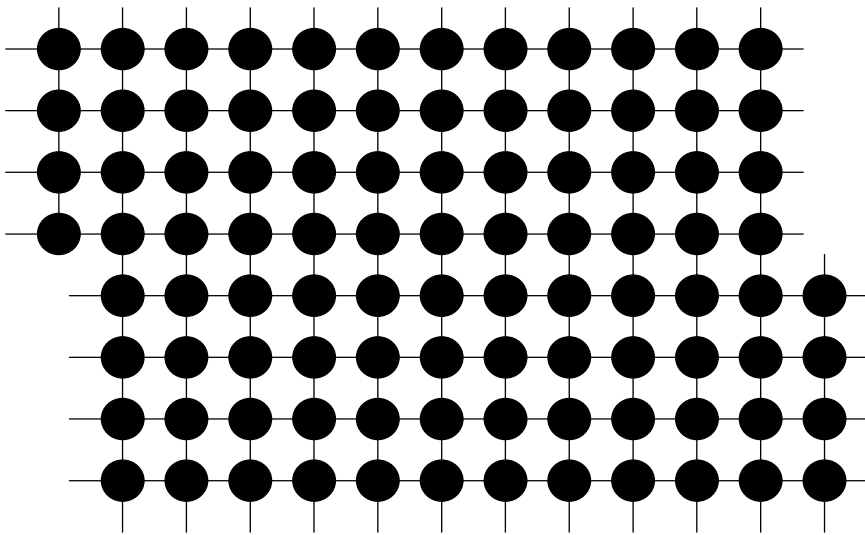




# Illustration of the Defects



# Dislocation Defects



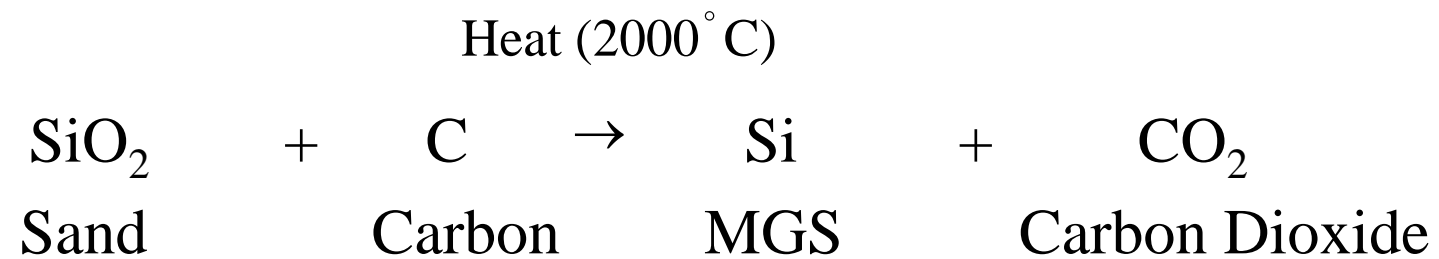
# From Sand to Wafer

- Quartz sand: silicon dioxide
- Sand to metallic grade silicon (MGS)
- React MGS powder with HCl to form TCS
- Purify TCS by vaporization and condensation
- React TCS to H<sub>2</sub> to form polysilicon (EGS)
- Melt EGS and pull single crystal ingot

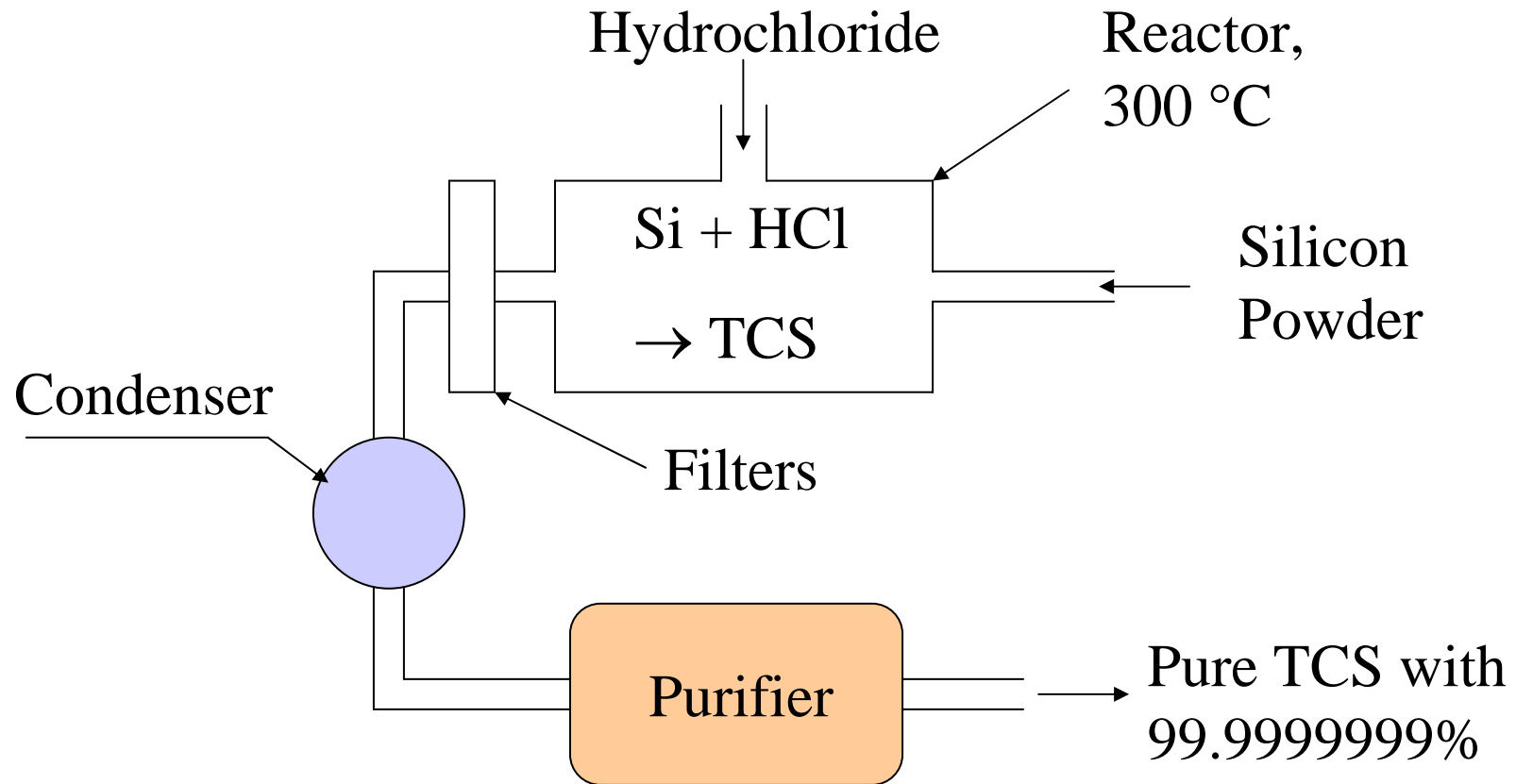
# From Sand to Wafer (cont.)

- Cut end, polish side, and make notch or flat
- Saw ingot into wafers
- Edge rounding, lap, wet etch, and CMP
- Laser scribe
  
- Epitaxy deposition

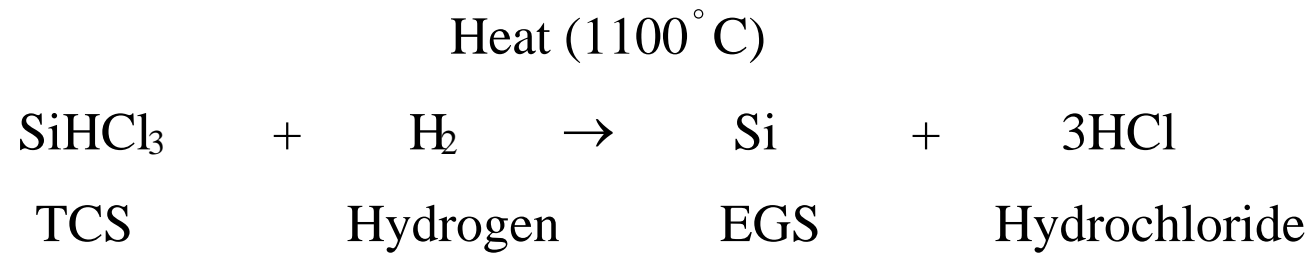
# From Sand to Silicon



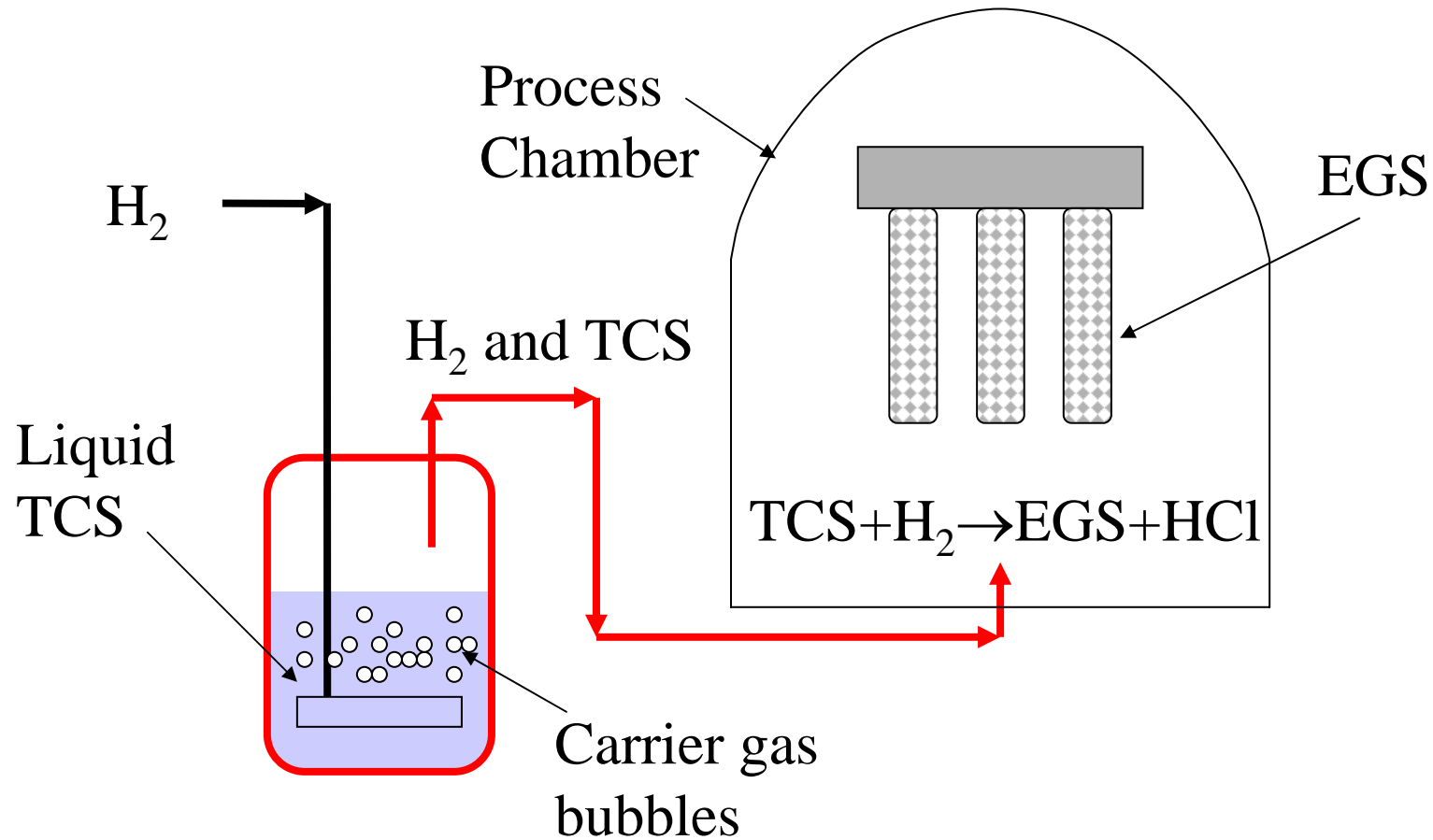
# Silicon Purification I



# Polysilicon Deposition, EGS

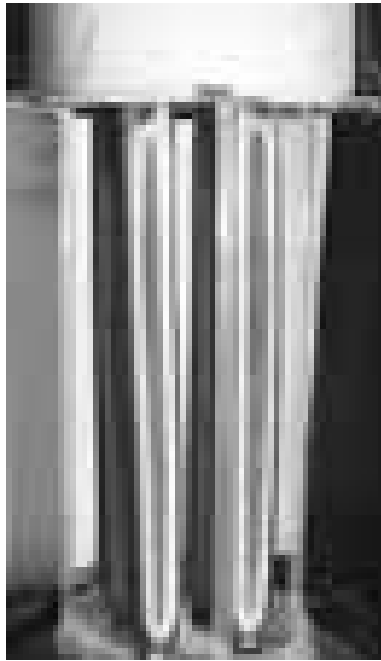


# Silicon Purification II



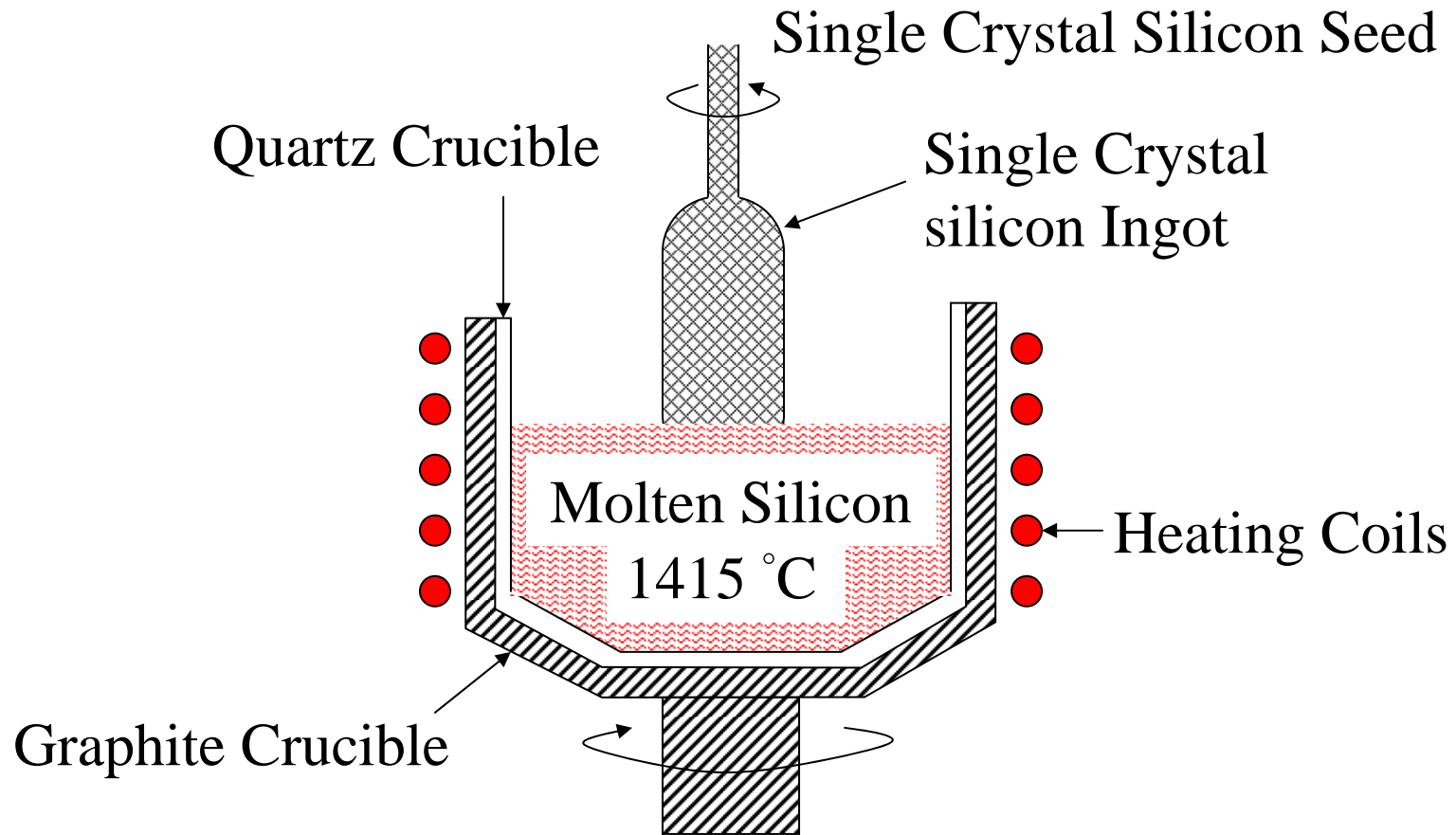


# Electronic Grade Silicon



Source: [http://www.fullman.com/semiconductors/\\_polysilicon.html](http://www.fullman.com/semiconductors/_polysilicon.html)

# Crystal Pulling: CZ method



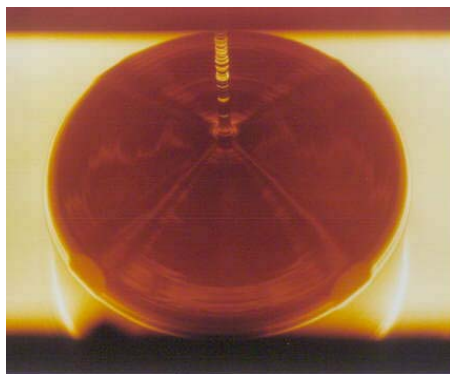
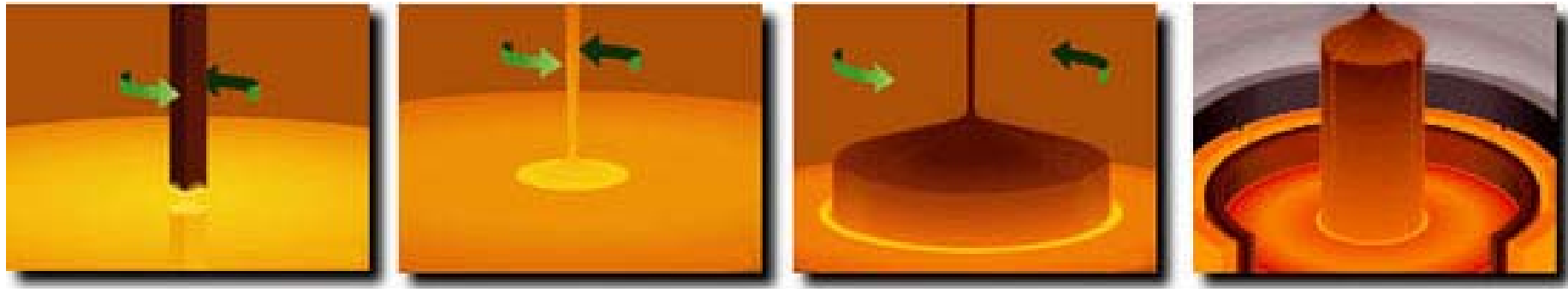
# CZ Crystal Pullers



## Mitsubishi Materials Silicon

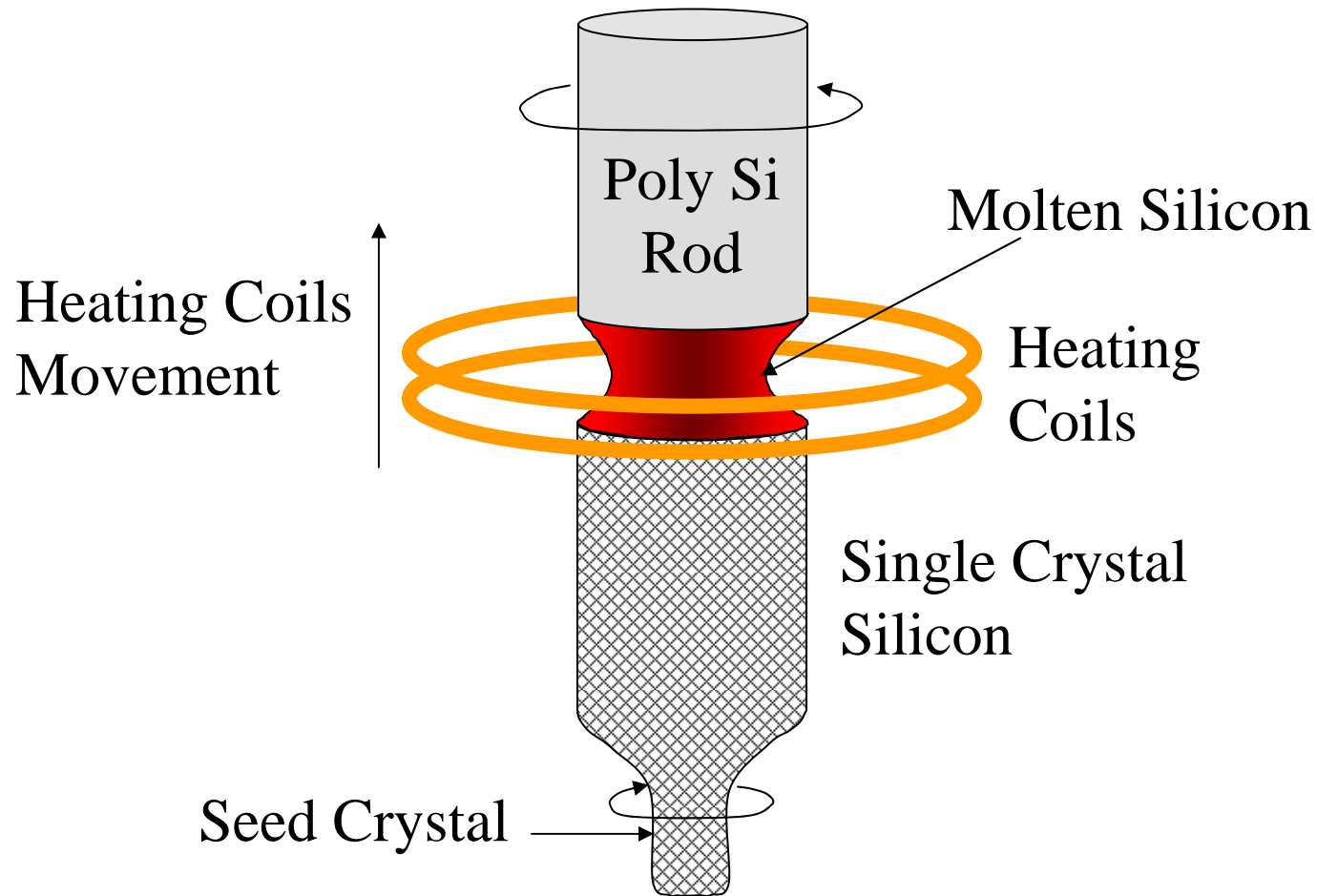
Source: [http://www.fullman.com/semiconductors/\\_crystalgrowing.html](http://www.fullman.com/semiconductors/_crystalgrowing.html)

# CZ Crystal Pulling



Source: [http://www.fullman.com/semiconductors/\\_crystalgrowing.html](http://www.fullman.com/semiconductors/_crystalgrowing.html)

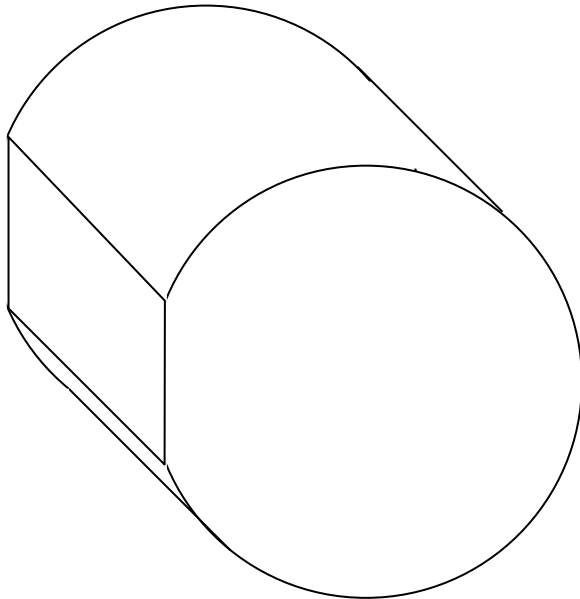
# Floating Zone Method



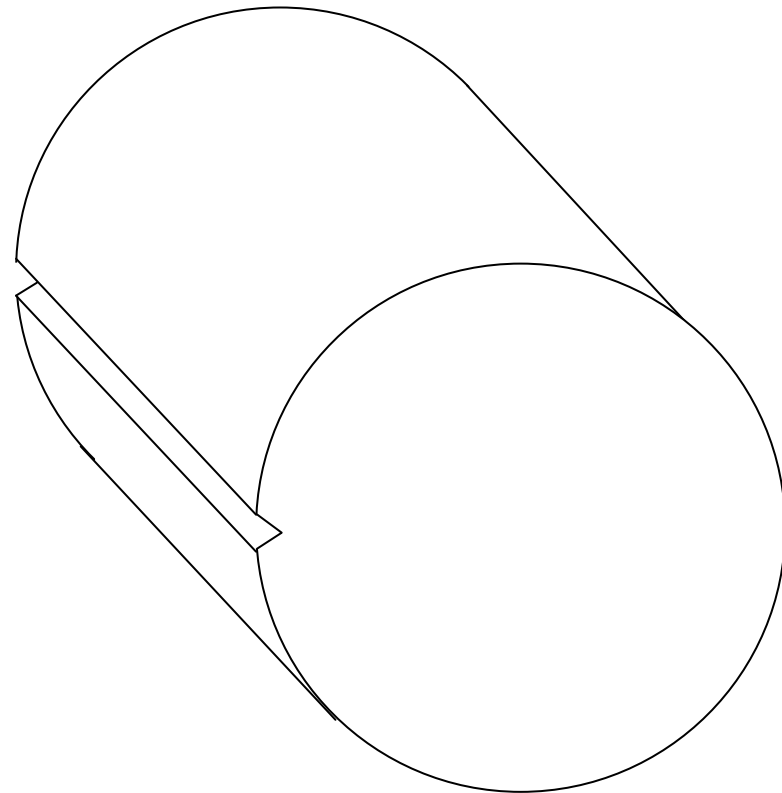
# Comparison of the Two Methods

- CZ method is more popular
  - Cheaper
  - Larger wafer size (300 mm in production)
  - Reusable materials
- Floating Zone
  - Pure silicon crystal (no crucible)
  - More expensive, smaller wafer size (150 mm)
  - Mainly for power devices.

# Ingot Polishing, Flat, or Notch

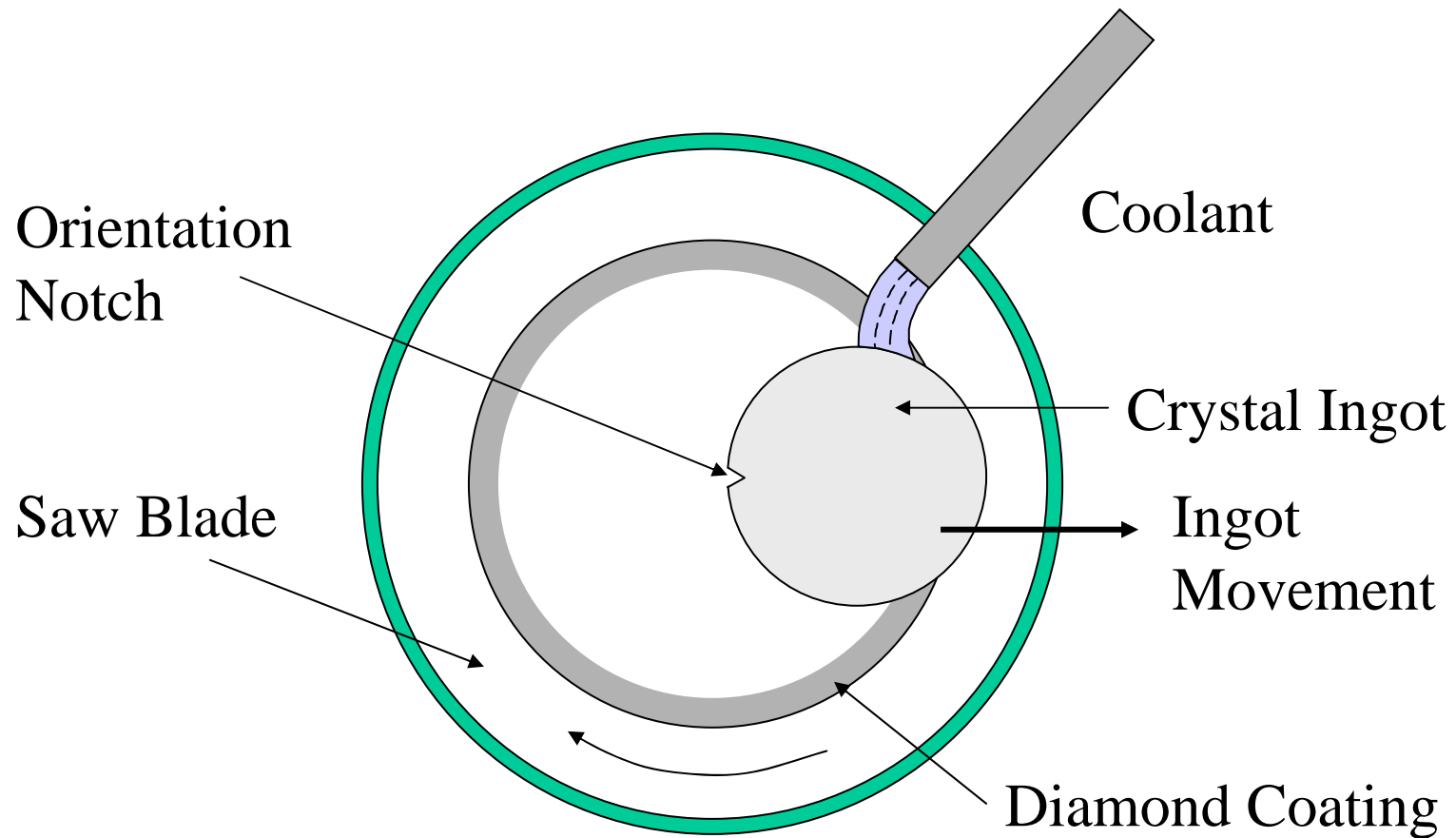


Flat, 150 mm and smaller



Notch, 200 mm and larger

# Wafer Sawing

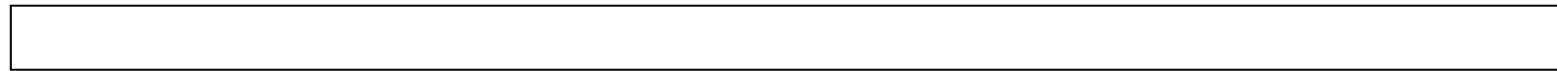
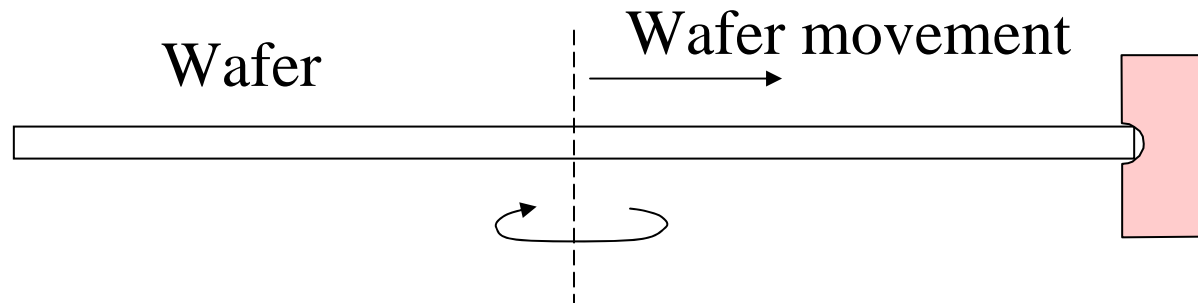




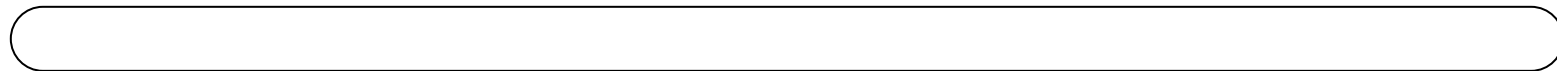
# Parameters of Silicon Wafer

<b>Wafer Size (mm)</b>	<b>Thickness (<math>\mu\text{m}</math>)</b>	<b>Area (<math>\text{cm}^2</math>)</b>	<b>Weight (grams)</b>
50.8 (2 in)	279	20.26	1.32
76.2 (3in)	381	45.61	4.05
100	525	78.65	9.67
125	625	112.72	17.87
150	675	176.72	27.82
200	725	314.16	52.98
300	775	706.21	127.62

# Wafer Edge Rounding



Wafer Before Edge Rounding



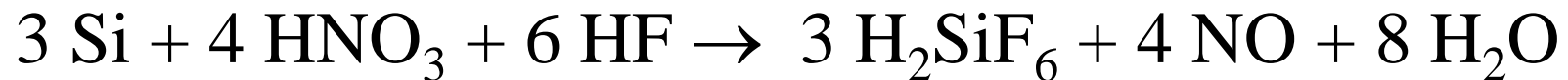
Wafer After Edge Rounding

# Wafer Lapping

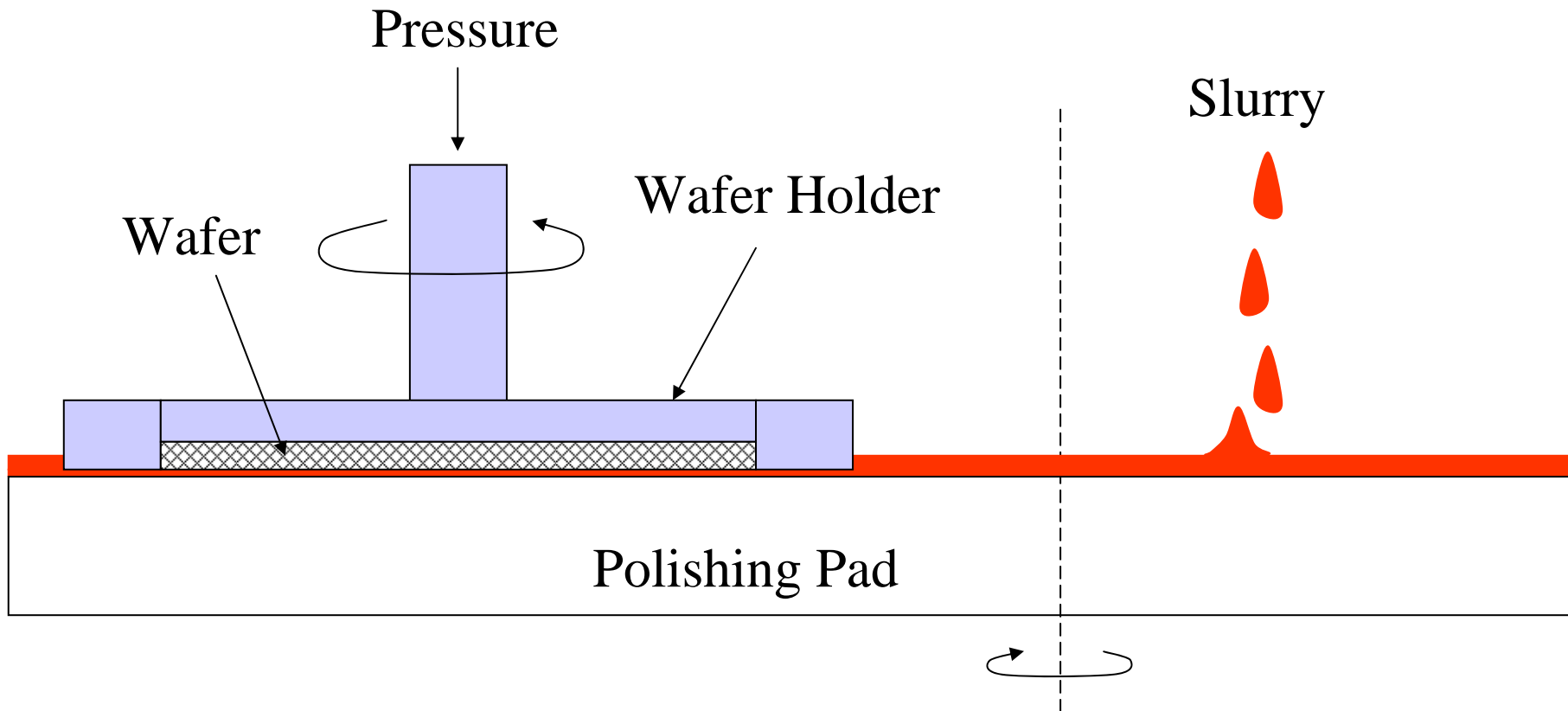
- Rough polished
- conventional, abrasive, slurry-lapping
- To remove majority of surface damage
- To create a flat surface

# Wet Etch

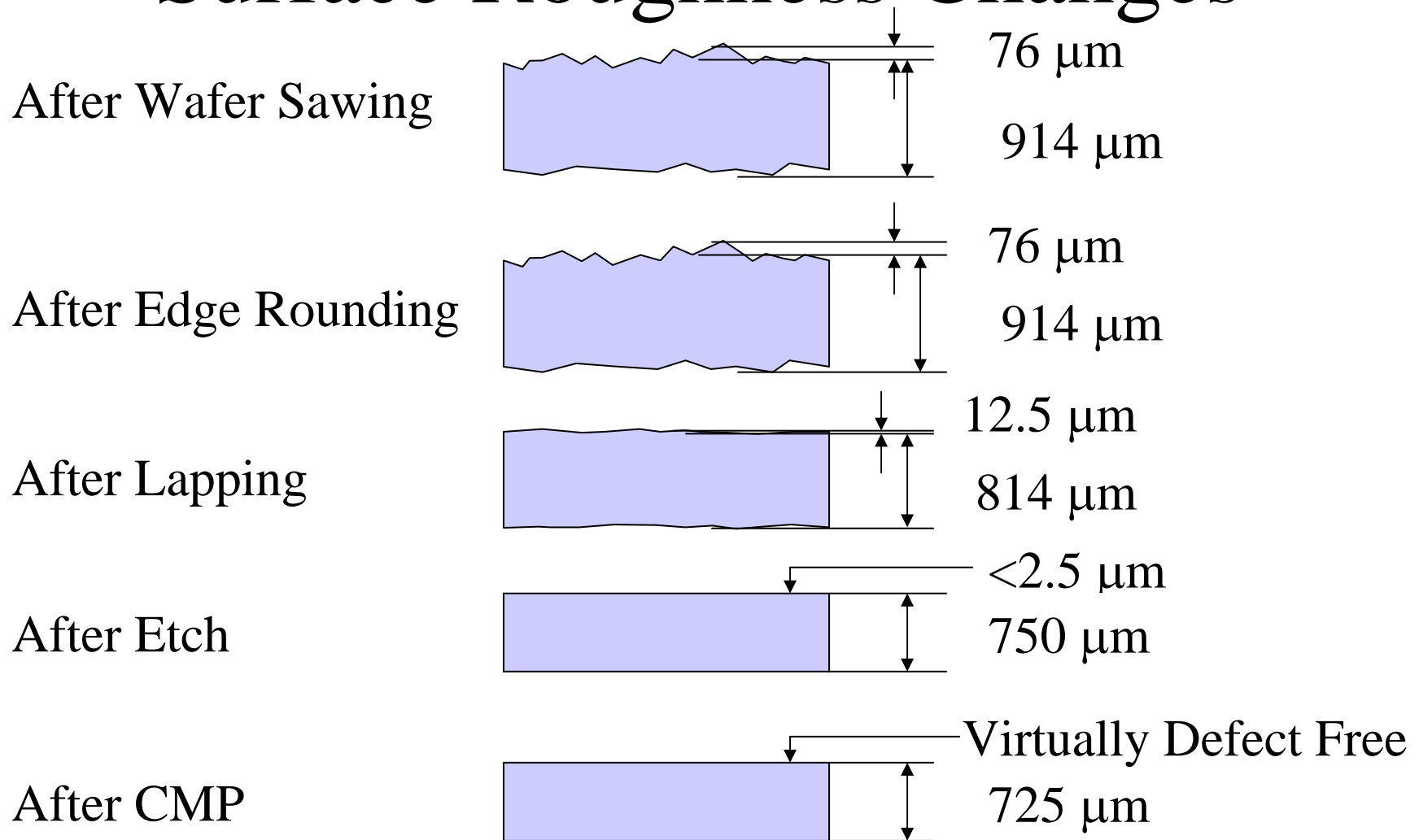
- Remove defects from wafer surface
- 4:1:3 mixture of HNO<sub>3</sub> (79 wt% in H<sub>2</sub>O), HF (49 wt% in H<sub>2</sub>O), and pure CH<sub>3</sub>COOH.
- Chemical reaction:



# Chemical Mechanical Polishing



# 200 mm Wafer Thickness and Surface Roughness Changes



# Epitaxy Grow

- Definition
- Purposes
- Epitaxy Reactors
- Epitaxy Process

# Epitaxy: Definition

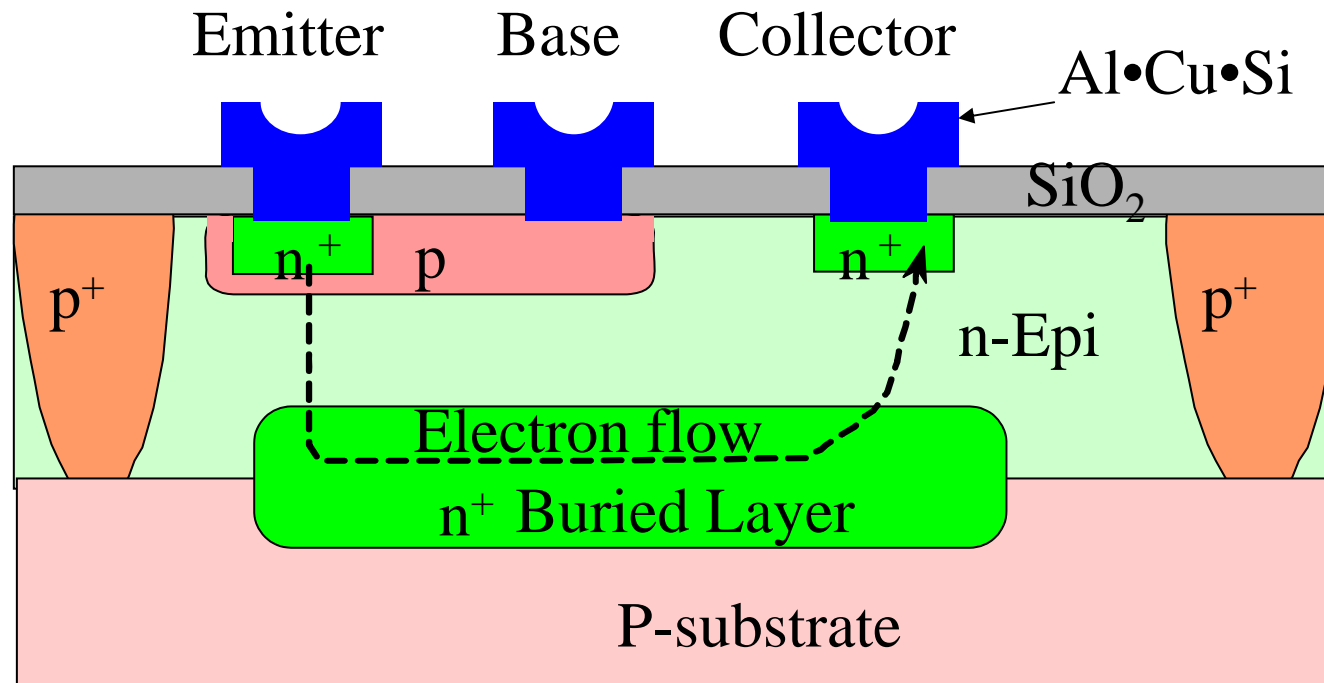
- Greek origin
- *epi*: upon
- *taxy*: orderly, arranged
  
- Epitaxial layer is a single crystal layer on a single crystal substrate.



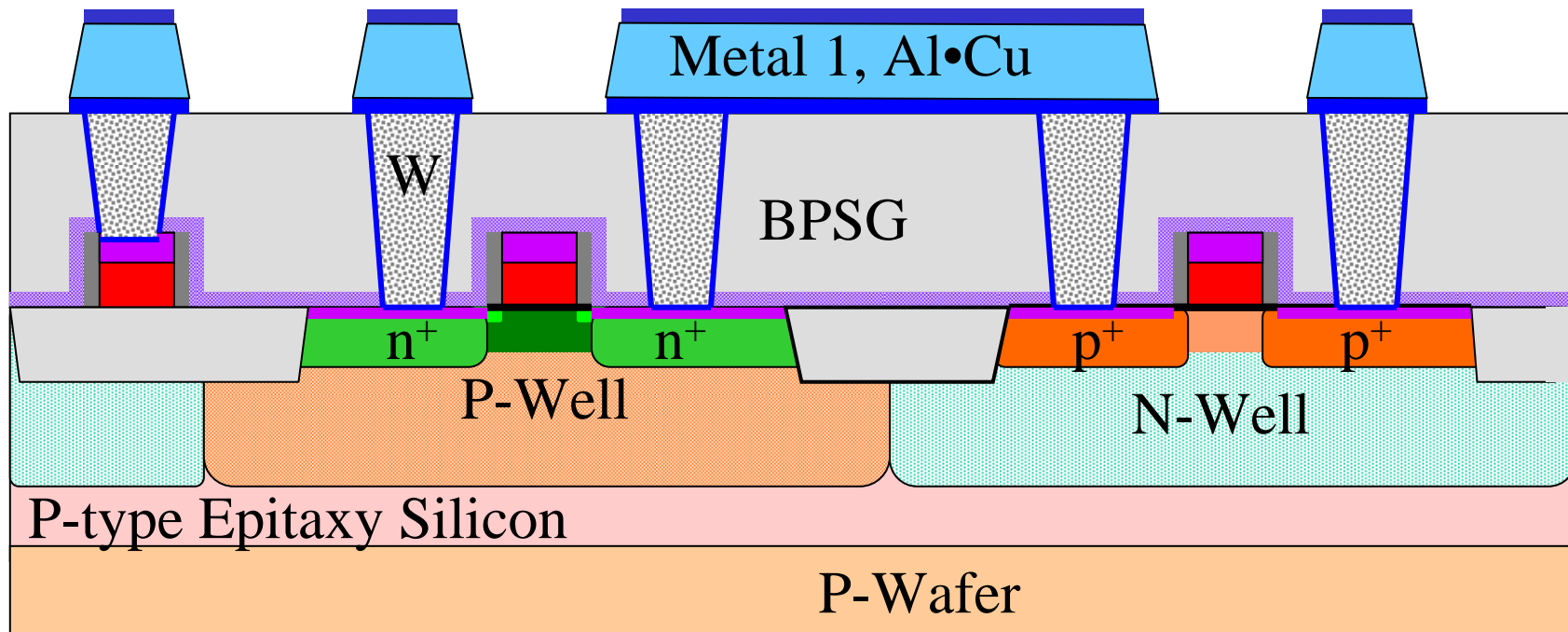
# Epitaxy: Purpose

- Barrier layer for bipolar transistor
  - Reduce collector resistance while keep high breakdown voltage.
  - Only available with epitaxy layer.
- Improve device performance for CMOS and DRAM because much lower oxygen, carbon concentration than the wafer crystal.

# Epitaxy Application, Bipolar Transistor



# Epitaxy Application: CMOS



# Silicon Source Gases

Silane



Dichlorosilane

DCS



Trichlorosilane

TCS

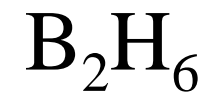


Tetrachlorosilane



# Dopant Source Gases

Diborane



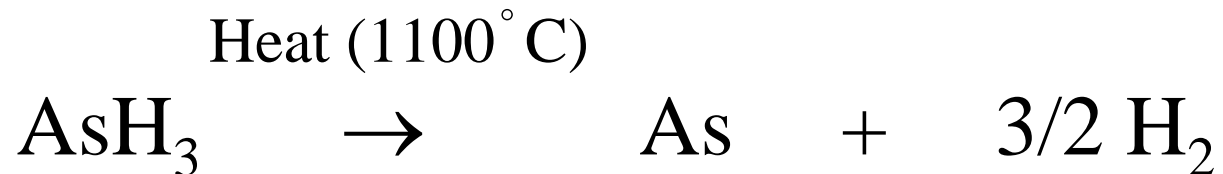
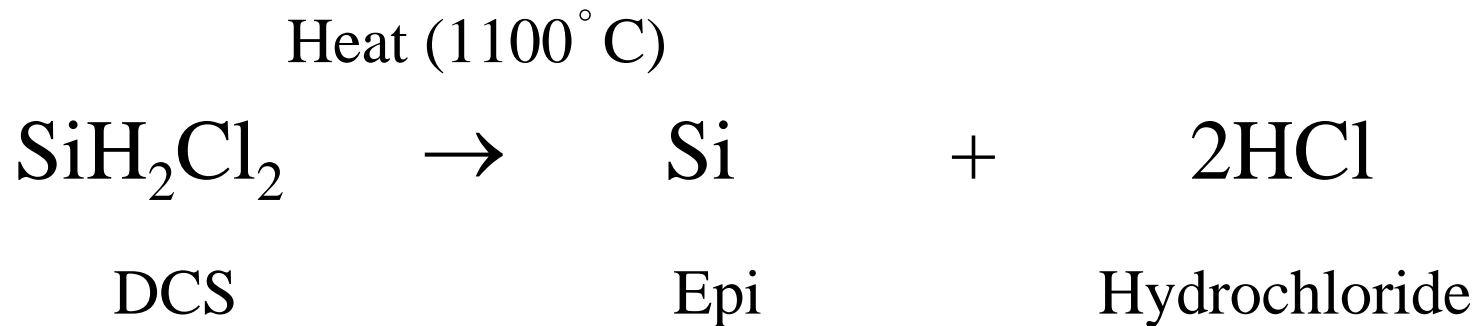
Phosphine



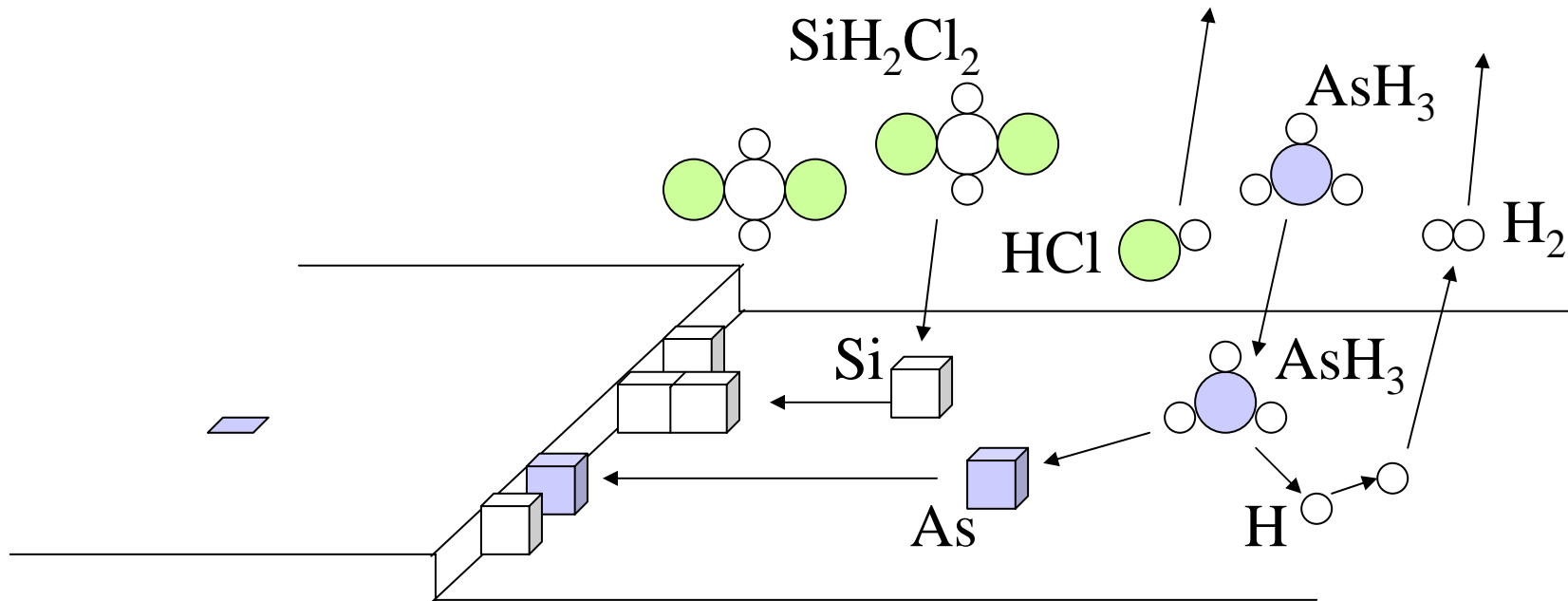
Arsine



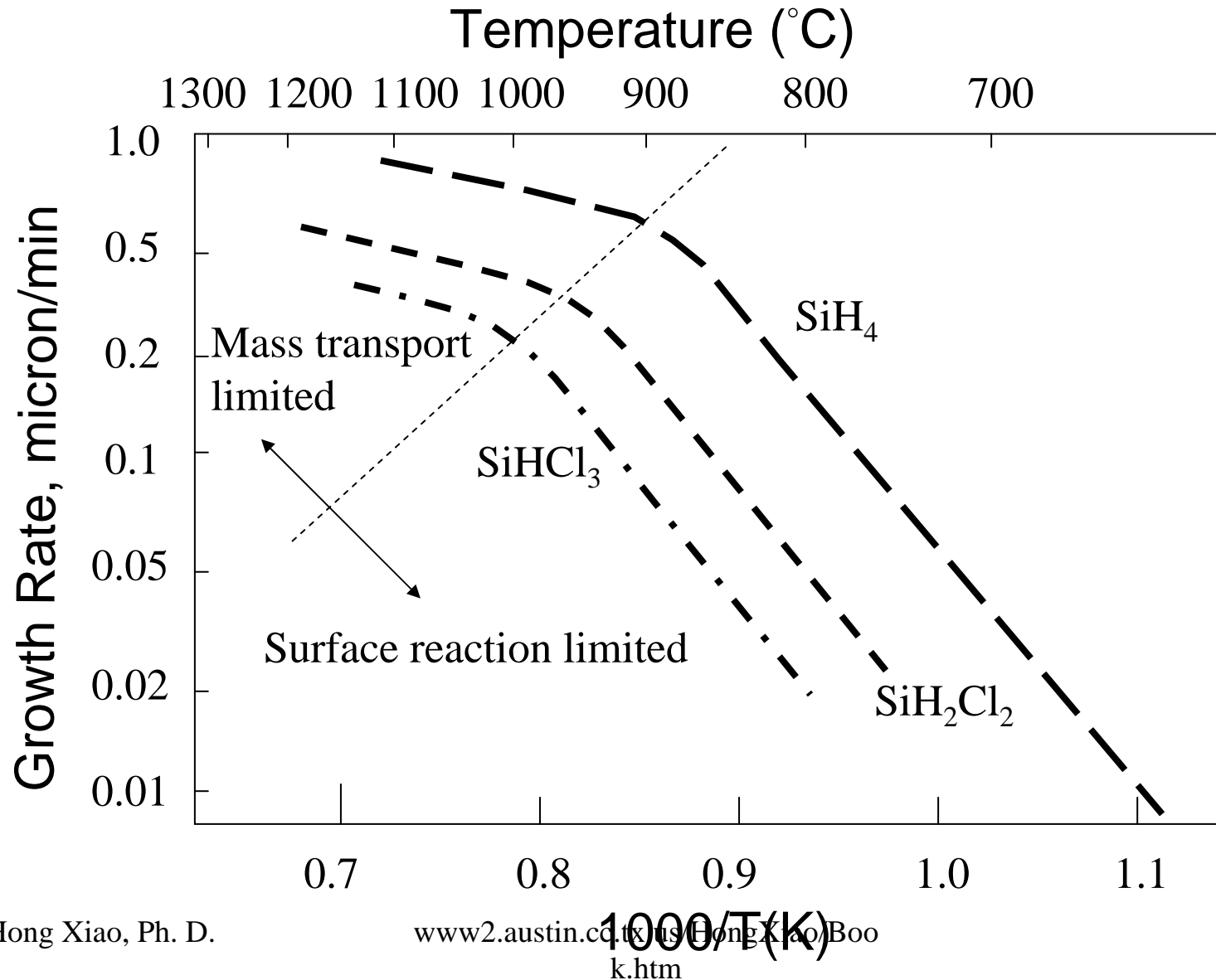
# DCS Epitaxy Grow, Arsenic Doping



# Schematic of DCS Epi Grow and Arsenic Doping Process

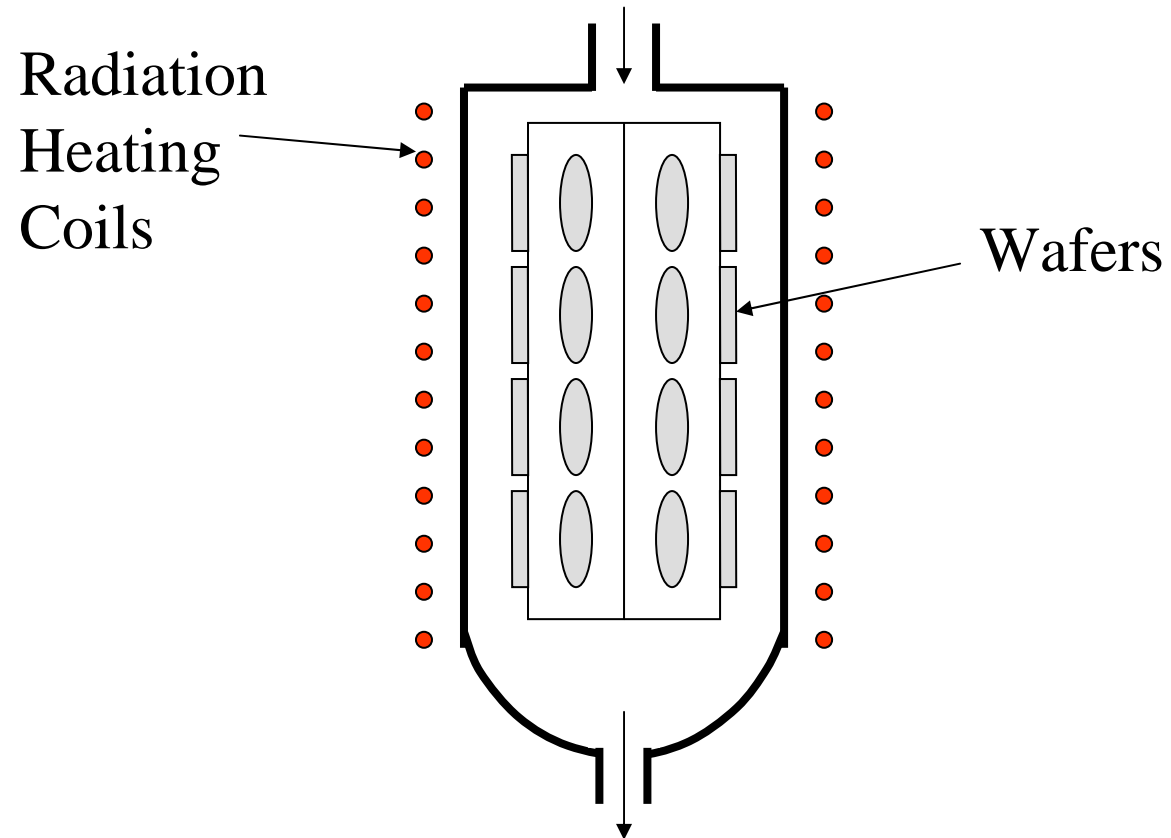


# Epitaxial Silicon Growth Rate Trends

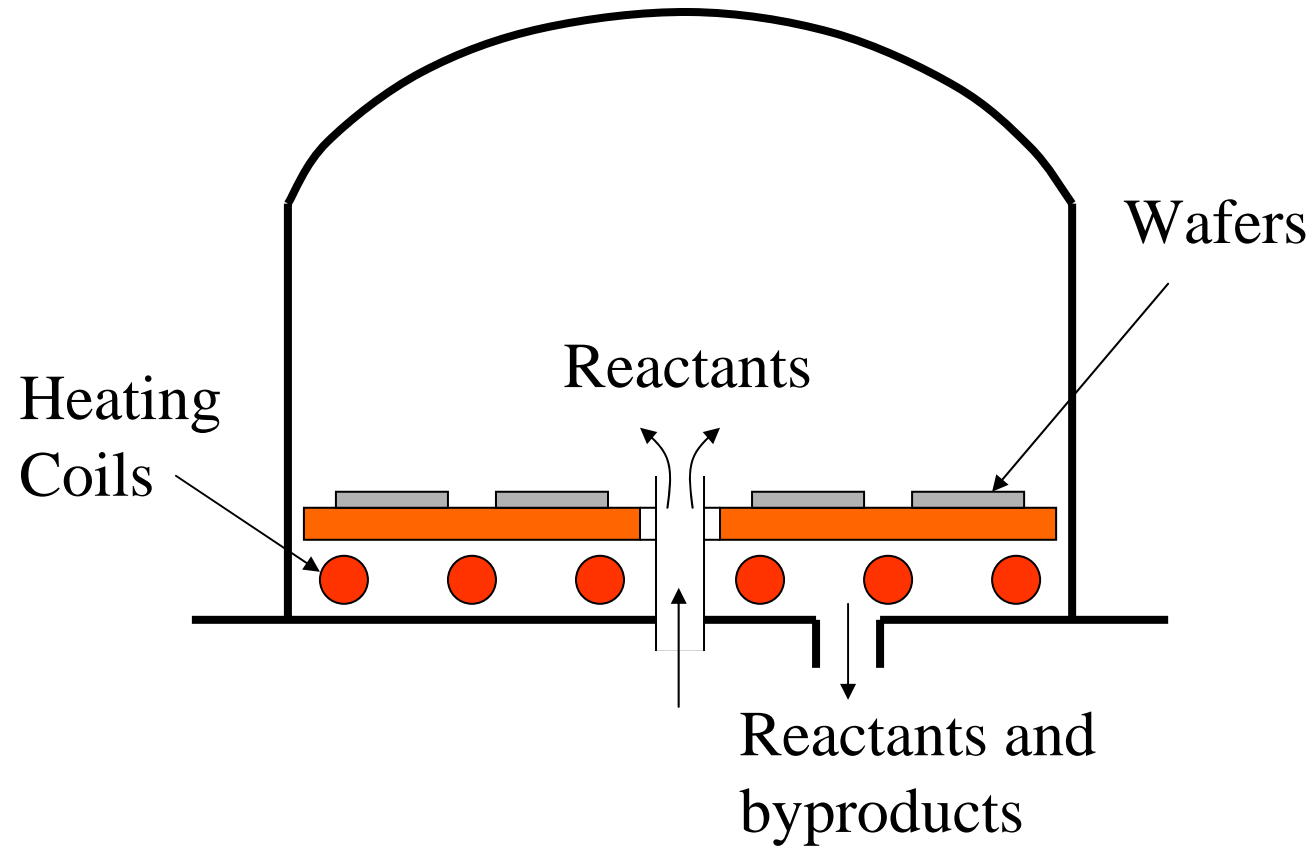




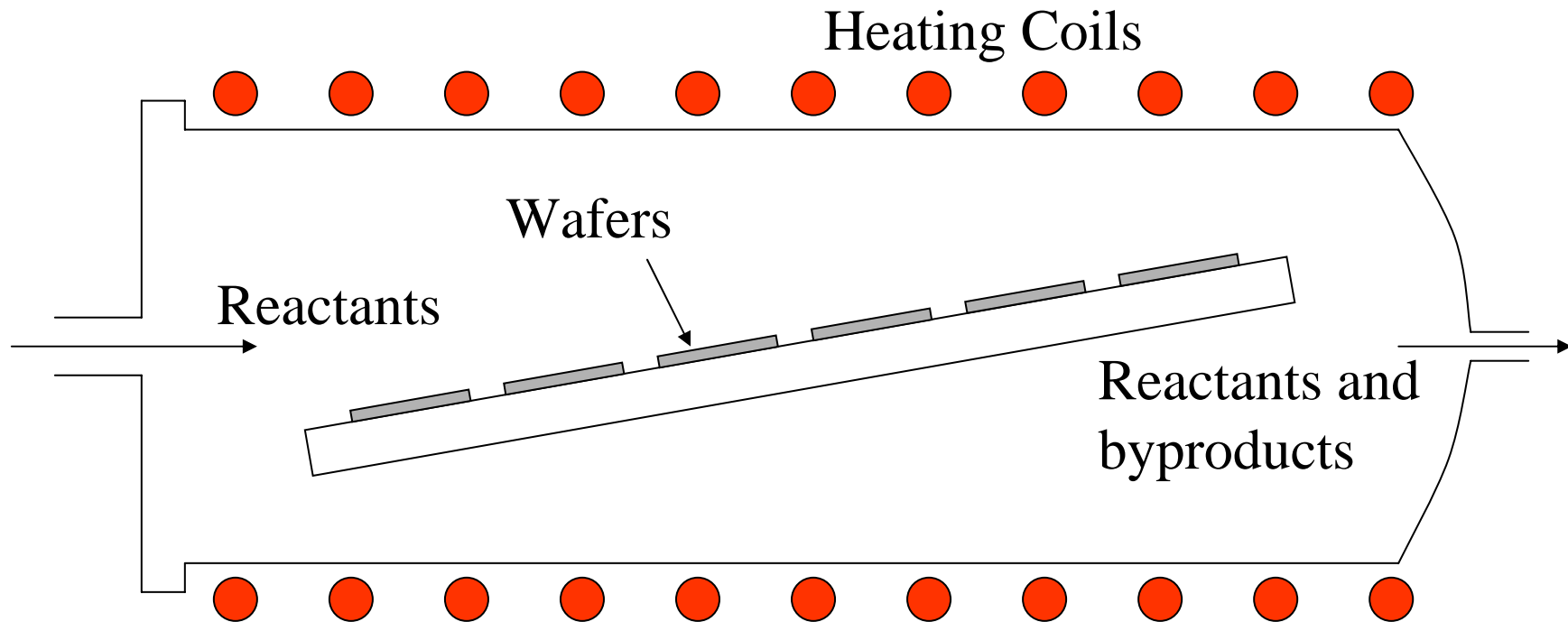
# Barrel Reactor



# Vertical Reactor



# Horizontal Reactor



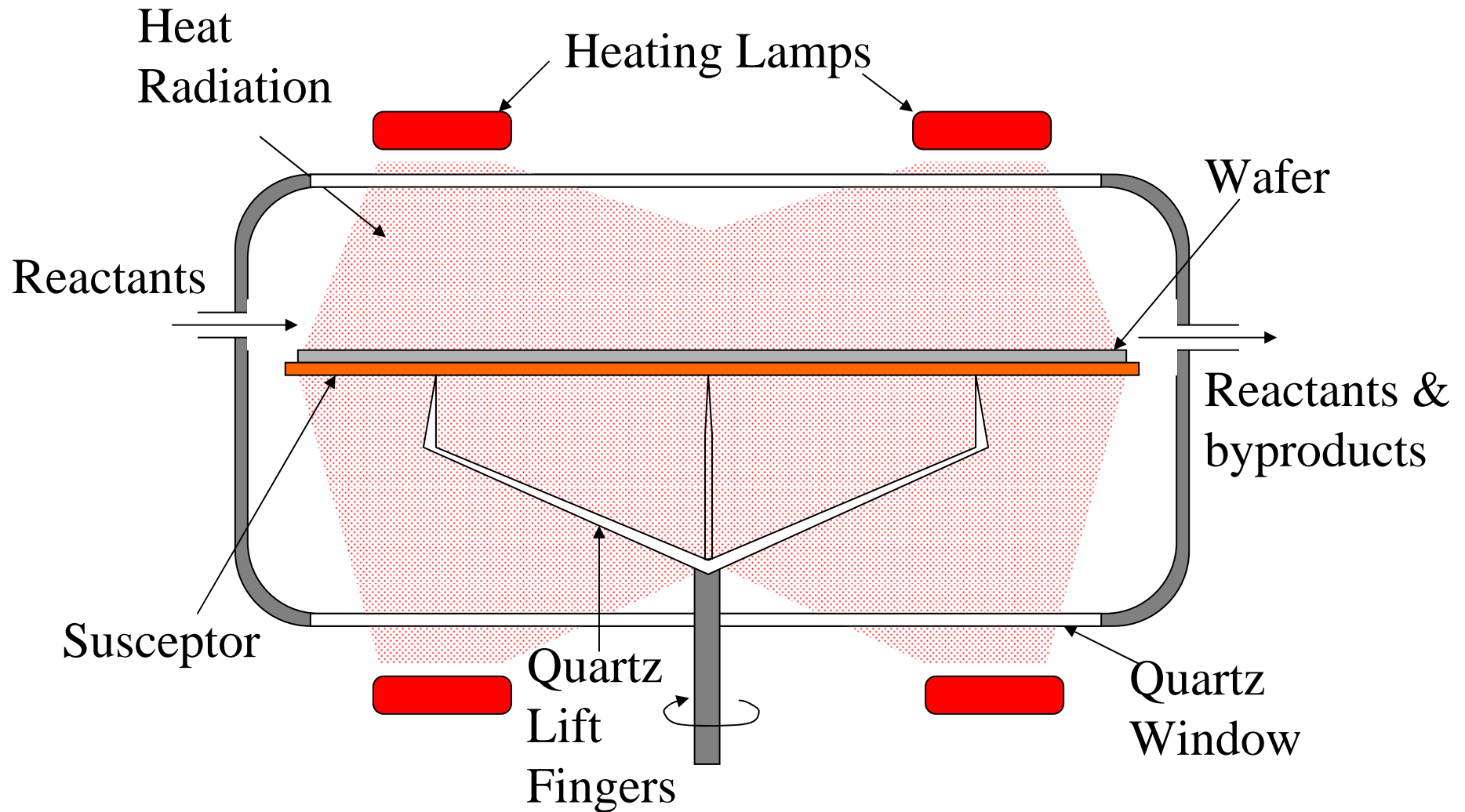
# Epitaxy Process, Batch System

- Hydrogen purge, temperature ramp up
- HCl clean
- Epitaxial layer grow
- Hydrogen purge, temperature cool down
- Nitrogen purge
- Open Chamber, wafer unloading, reloading

# Single Wafer Reactor

- Sealed chamber, hydrogen ambient
- Capable for multiple chambers on a mainframe
- Large wafer size (to 300 mm)
- Better uniformity control

# Single Wafer Reactor



# Epitaxy Process, Single Wafer System

- Hydrogen purge, clean, temperature ramp up
- Epitaxial layer grow
- Hydrogen purge, heating power off
- Wafer unloading, reloading
  
- In-situ HCl clean,

# Why Hydrogen Purge

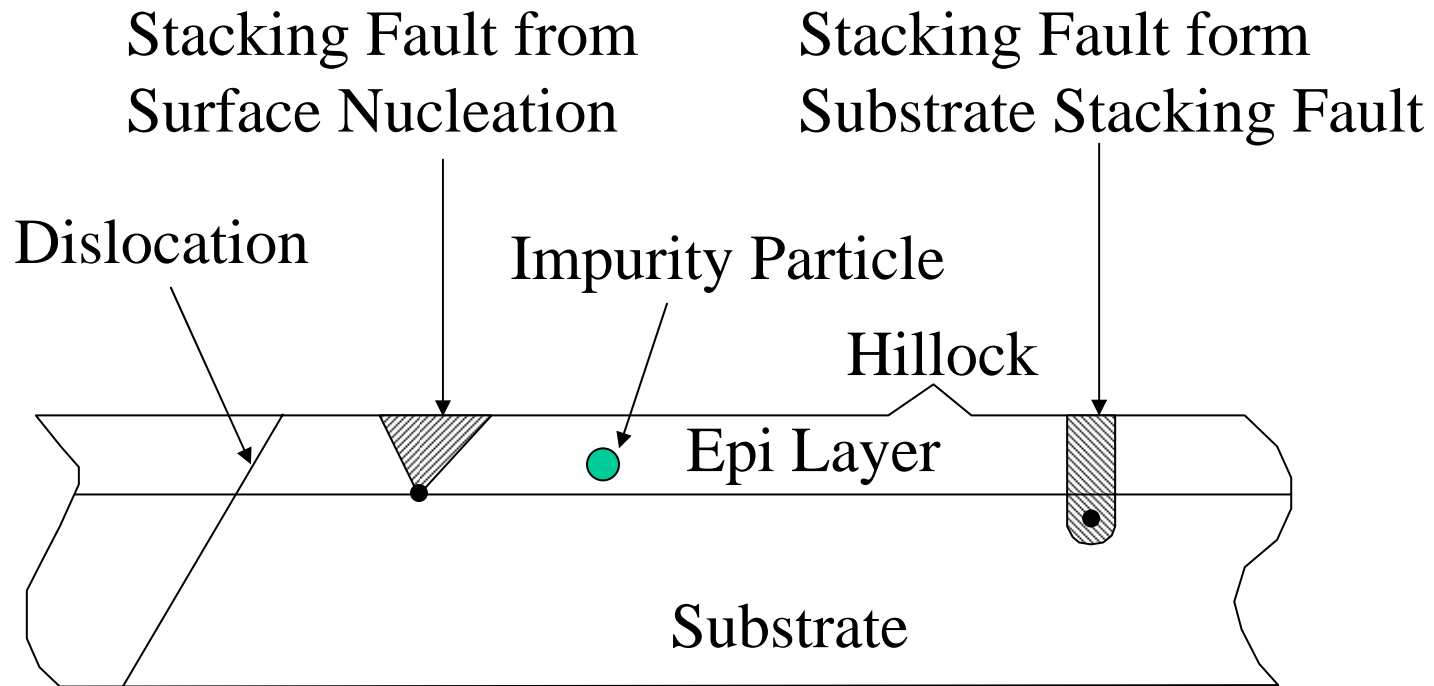
- Most systems use nitrogen as purge gas
- Nitrogen is a very stable abundant
- At  $> 1000$  °C,  $N_2$  can react with silicon
- SiN on wafer surface affects epi deposition
- $H_2$  is used for epitaxy chamber purge
- Clean wafer surface by hydrides formation



# Properties of Hydrogen

Name	Hydrogen
Symbol	H
Atomic number	1
Atomic weight	1.00794
Discoverer	Henry Cavendish
Discovered at	England
Discovery date	1766
Origin of name	From the Greek words "hydro" and "genes" meaning "water" and "generator"
Molar volume	11.42 cm <sup>3</sup>
Velocity of sound	1270 m/sec
Refractive index	1.000132
Melting point	-258.99 C
Boiling point	-252.72 C
Thermal conductivity	0.1805 W m <sup>-1</sup> K <sup>-1</sup>

# Defects in Epitaxy Layer



After S.M. Zse's *VLSI Technology*

# Future Trends

- Larger wafer size
- Single wafer epitaxial grow
- Low temperature epitaxy
- Ultra high vacuum (UHV, to  $10^{-9}$  Torr)
- Selective epitaxy

# Summary

- Silicon is abundant, cheap and has strong, stable and easy grown oxide.
- $\langle 100 \rangle$  and  $\langle 111 \rangle$
- CZ and floating zone, CZ is more popular
- Sawing, edging, lapping, etching and CMP

# Summary

- Epitaxy: single crystal on single crystal
- Needed for bipolar and high performance CMOS, DRAM.
- Silane, DCS, TCS as silicon precursors
- $B_2H_6$  as P-type dopant
- $PH_3$  and  $AsH_3$  as N-type dopants
- Batch and single wafer systems