Chapter 2
Introduction of IC Fabrication

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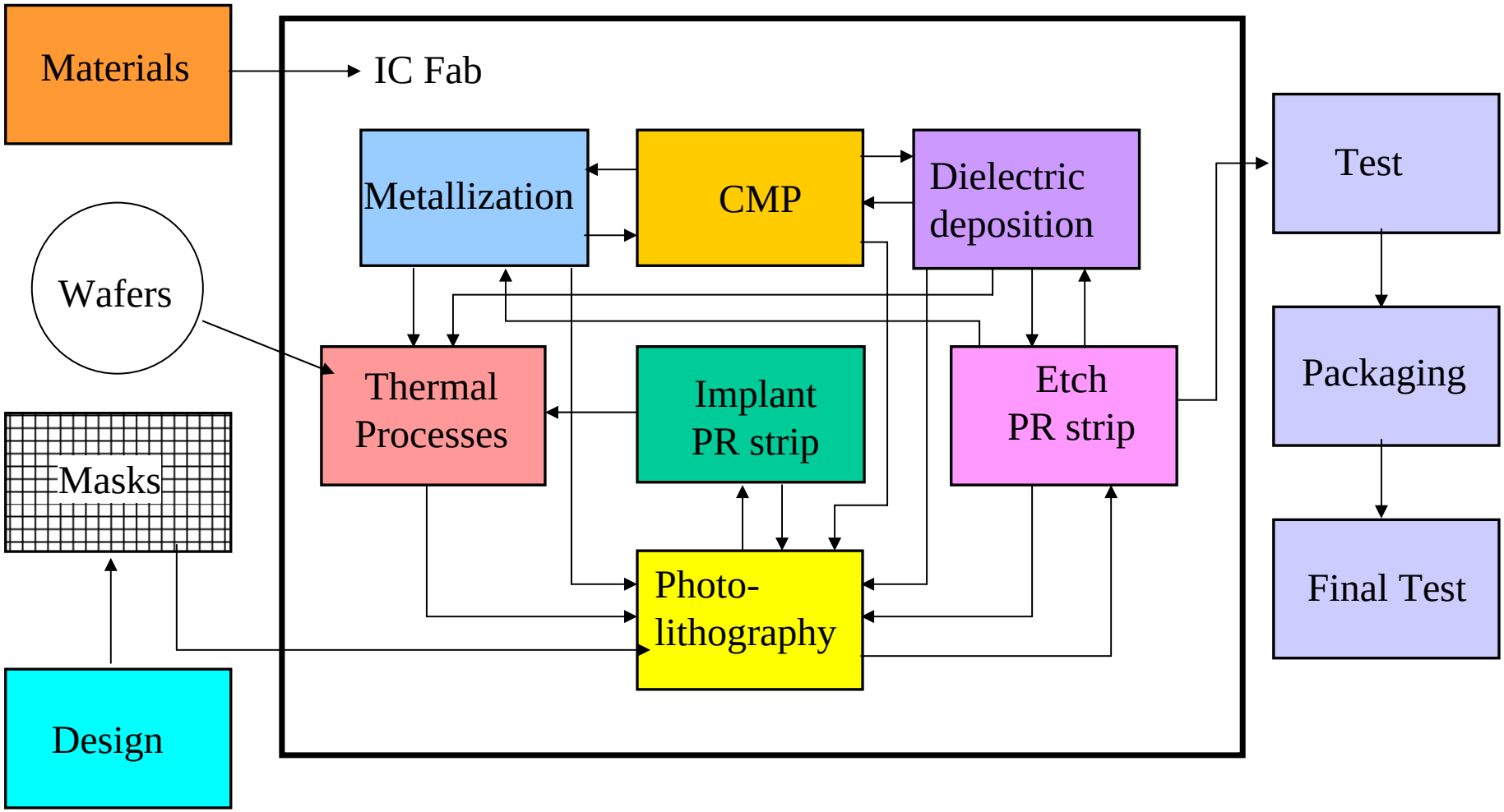
Objectives

- Define yield and explain its importance
- Describe the basic structure of a cleanroom.
- Explain the importance of cleanroom protocols
- List four basic operations of IC processing
- Name at least six process bays in an IC fab
- Explain the purposes of chip packaging
- Describe the standard wire bonding and flip-chip bump bonding processes

Wafer Process Flow



Fab Cost

- Fab cost is very high, > $1B for 8” fab
- Clean room
- Equipment, usually > $1M per tool
- Materials, high purity, ultra high purity
- Facilities
- People, training and pay

Wafer Yield

$$Y_W = \frac{Wafers_{good}}{Wafers_{total}}$$

Die Yield

$$Y_D = \frac{Dies_{good}}{Dies_{total}}$$

Packaging Yield

$$Y_C = \frac{Chips_{good}}{Chips_{total}}$$

Overall Yield

$$Y_T = Y_W \times Y_D \times Y_C$$

Overall Yield determines whether a fab is making profit or losing money

How Does Fab Make (Loss) Money

- Cost:
  - Wafer (8”): ~$150/wafer*
  - Processing: ~$1200 ($2/wafer/step, 600 steps)
  - Packing: ~$5/chip
- Sale:
  - ~200 chips/wafer
  - ~$50/chip (low-end microprocessor in 2000)

*Cost of wafer, chips per wafer, and price of chip varies, numbers here are choosing randomly based on general information.

How Does a Fab Make (*Loss*) Money

Cost:	• **100% yield: 150+1200+1000 = $2350/wafer** • 50% yield: 150+1200+500 = $1850/wafer • *0% yield: 150+1200 = $1350/wafer*
Sale:	• **100% yield: 200×50 = $10,000/wafer** • 50% yield: 100×50 = $5,000/wafer • *0% yield: 0×50 = $0.00/wafer*
Profit Margin:	• **100% yield: 10000 – 2350 = $7650/wafer** • 50% yield : 5000 – 1850 = $3150/wafer • *0% yield : 0 – 1350 = – $1350/wafer*

Question

- If yield for every process step is 99%, what is the overall processing yield after 600 process steps?

Answer

- It equals to 99% times 99% 600 times
- $0.99^{600} = 0.0024 = 0.24\%$
- Almost no yield

Throughput

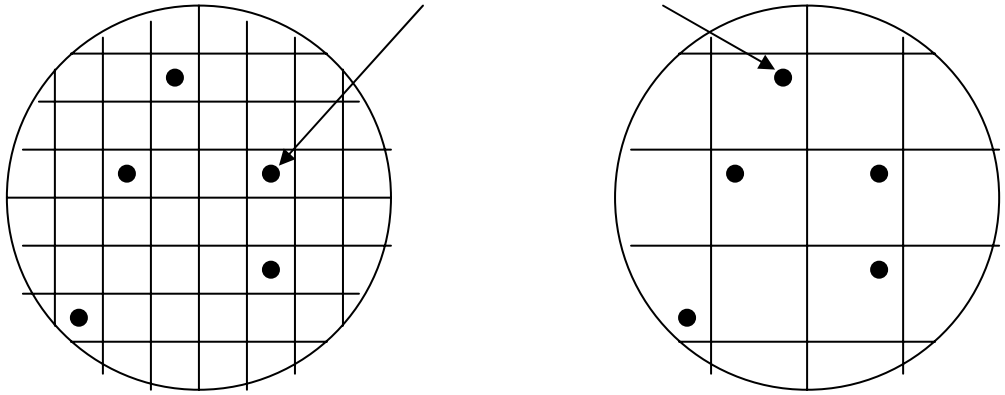
- Number of wafers able to process
  - Fab: wafers/month (typically 10,000)
  - Tool: wafers/hour (typically 60)
- At high yield, high throughput brought

Defects and Yield

$$Y \propto \frac{1}{(1+DA)^n}$$

Yield and Die Size

Killer Defects



$Y = 28/32 = 87.5\%$ $Y = 2/6 = 33.3\%$

Illustration of a Production Wafer

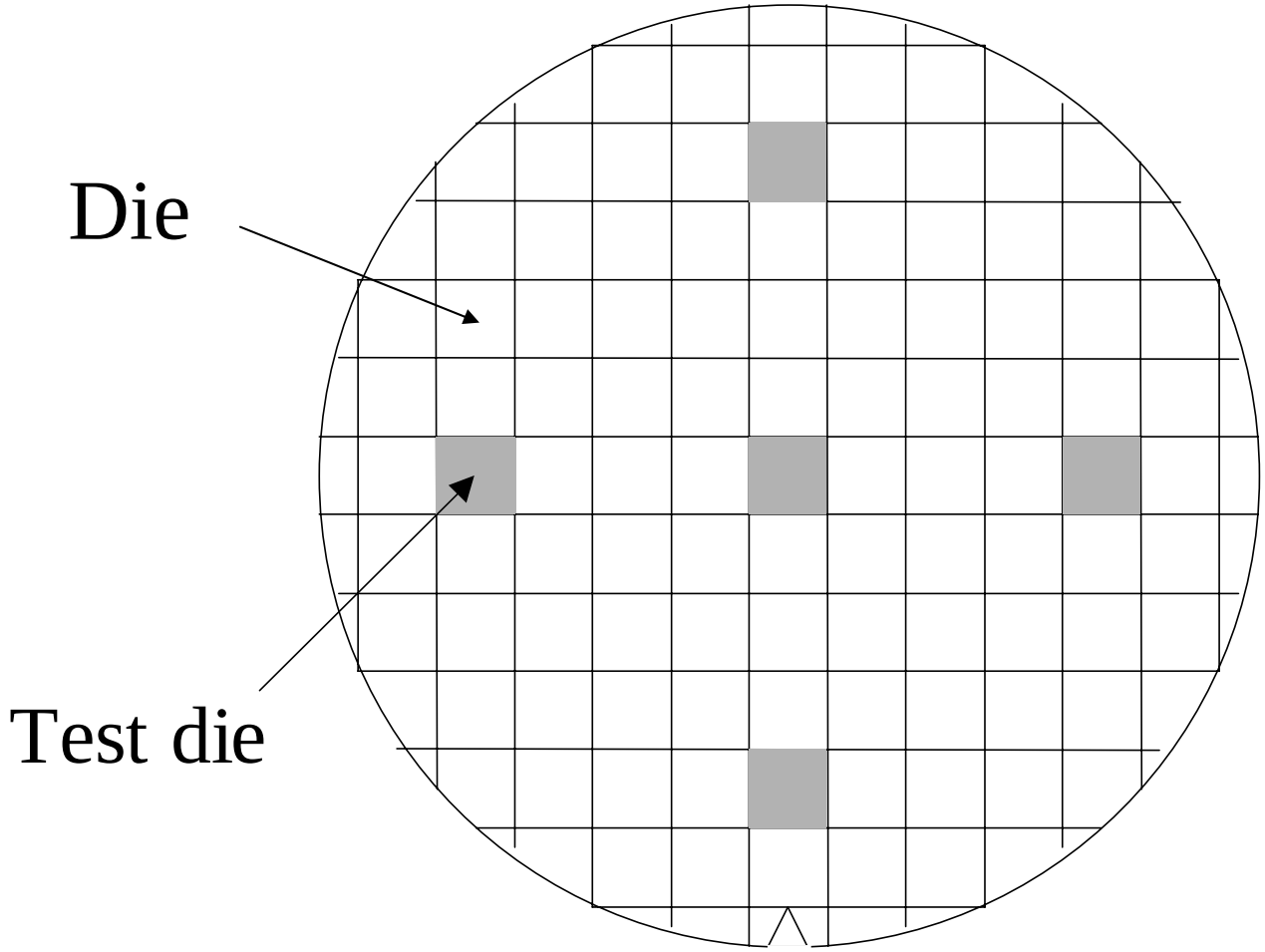
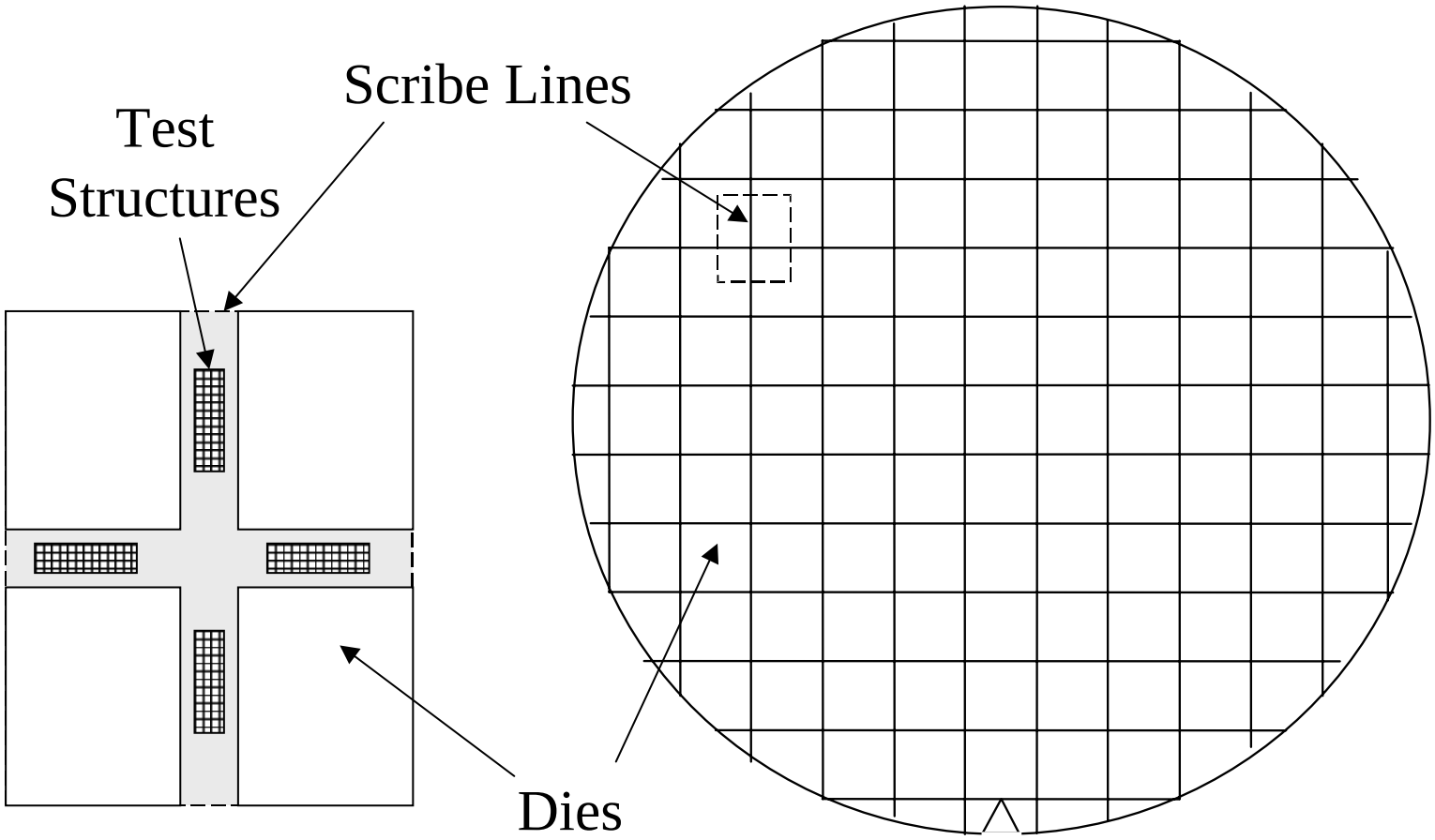


Illustration of a Production Wafer



Clean Room

- Artificial environment with low particle counts
- Started in medical application for post-surgery infection prevention

- Particles kills yield
- IC fabrication must in a clean room

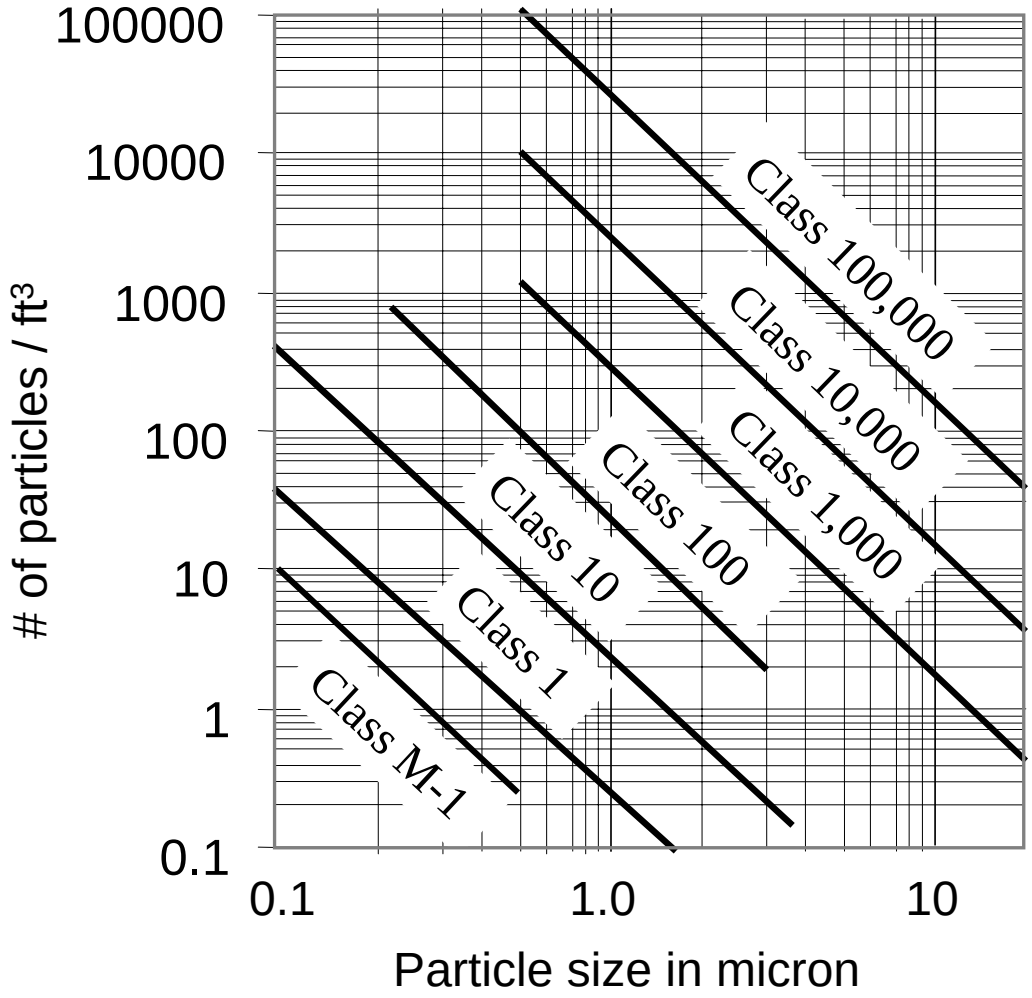
Clean Room

- First used for surgery room to avoid bacteria contamination
- Adopted in semiconductor industry in 1950
- Smaller device needs higher grade clean room
- Less particle, more expensive to build

Clean Room Class

- Class 10 is defined as less than 10 particles with diameter larger than 0.5 μm per cubic foot.
- Class 1 is defined as less than 1 such particles per cubic foot.
- 0.18 mm device require higher than Class 1 grade clean room.

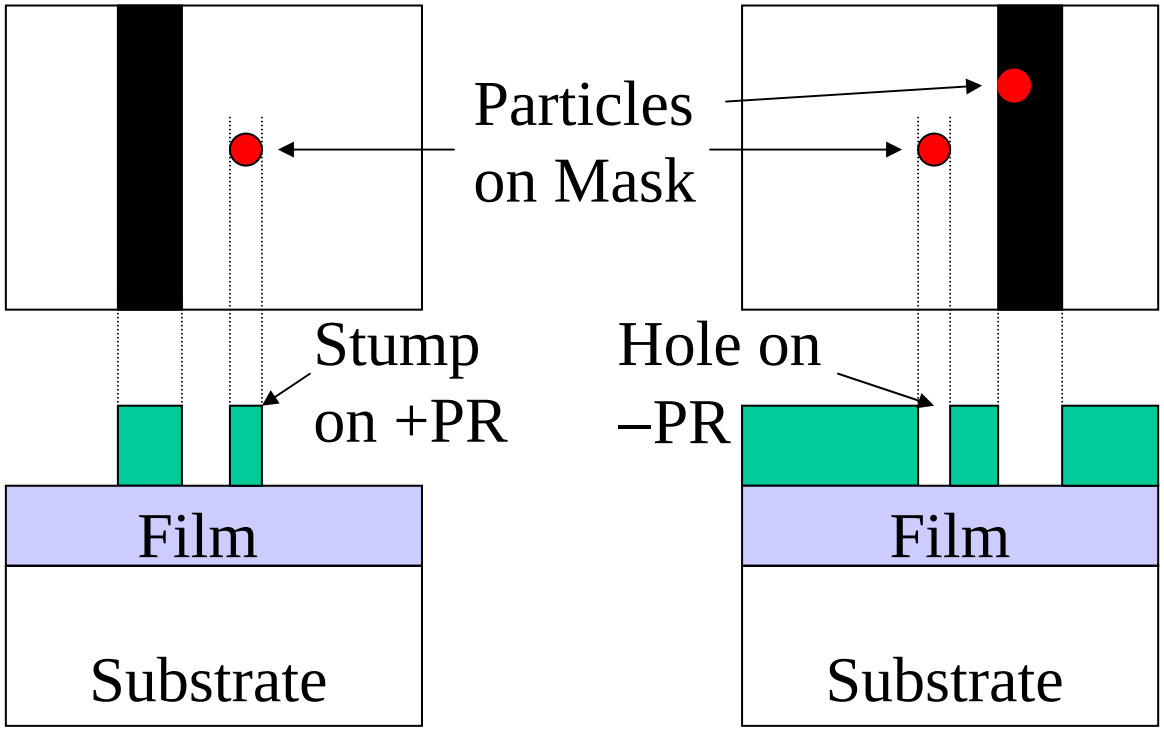
Cleanroom Classes



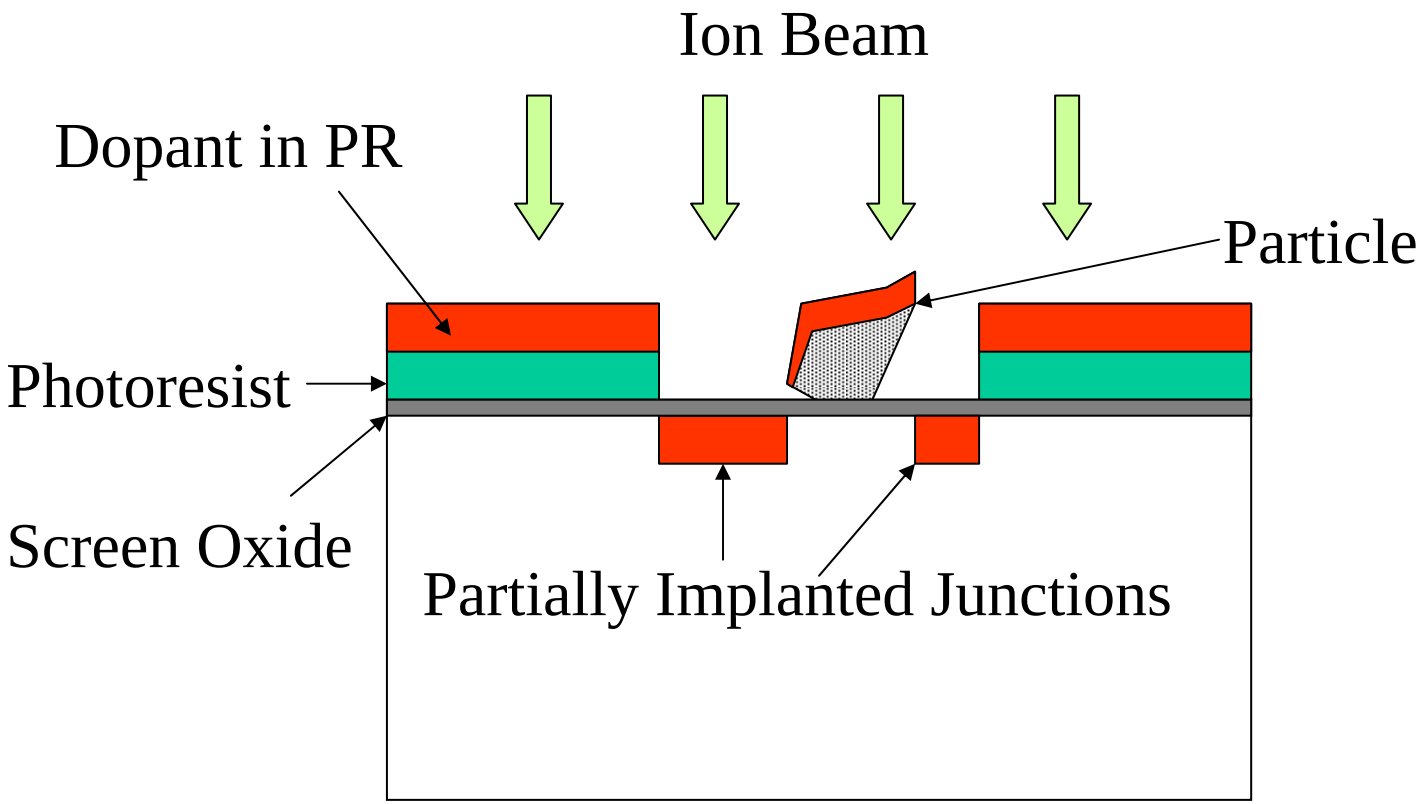
Definition of Airborne Particulate Cleanliness Class per Fed. Std. 209E

Class	Particles/ft^3				
	0.1 μm	0.2 μm	0.3 μm	0.5 μm	5 μm
M-1	9.8	2.12	0.865	0.28	
1	35	7.5	3	1	
10	350	75	30	10	
100		750	300	100	
1000				1000	7
10000				10000	70

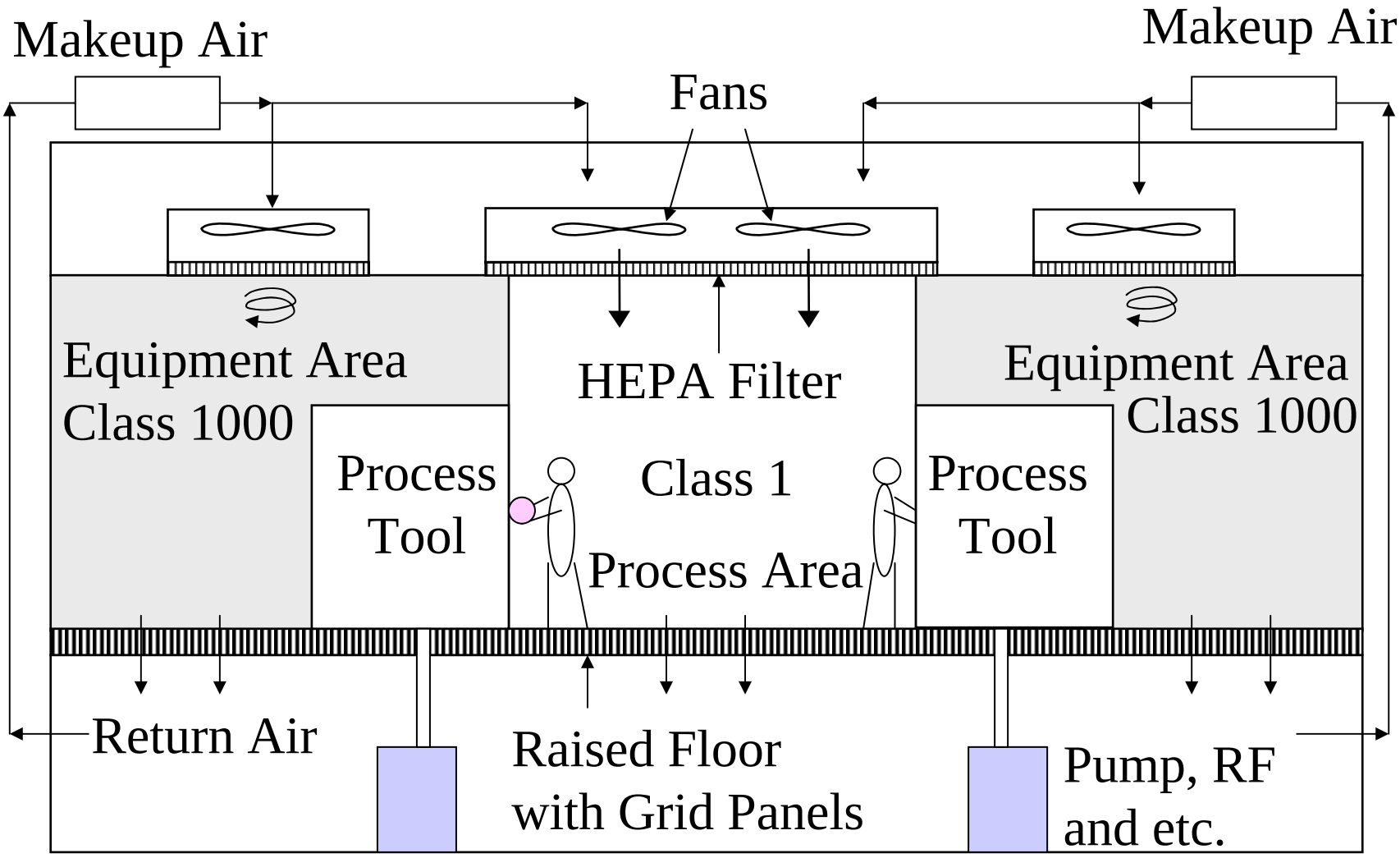
Effect of Particles on Masks



Effect of Particle Contamination



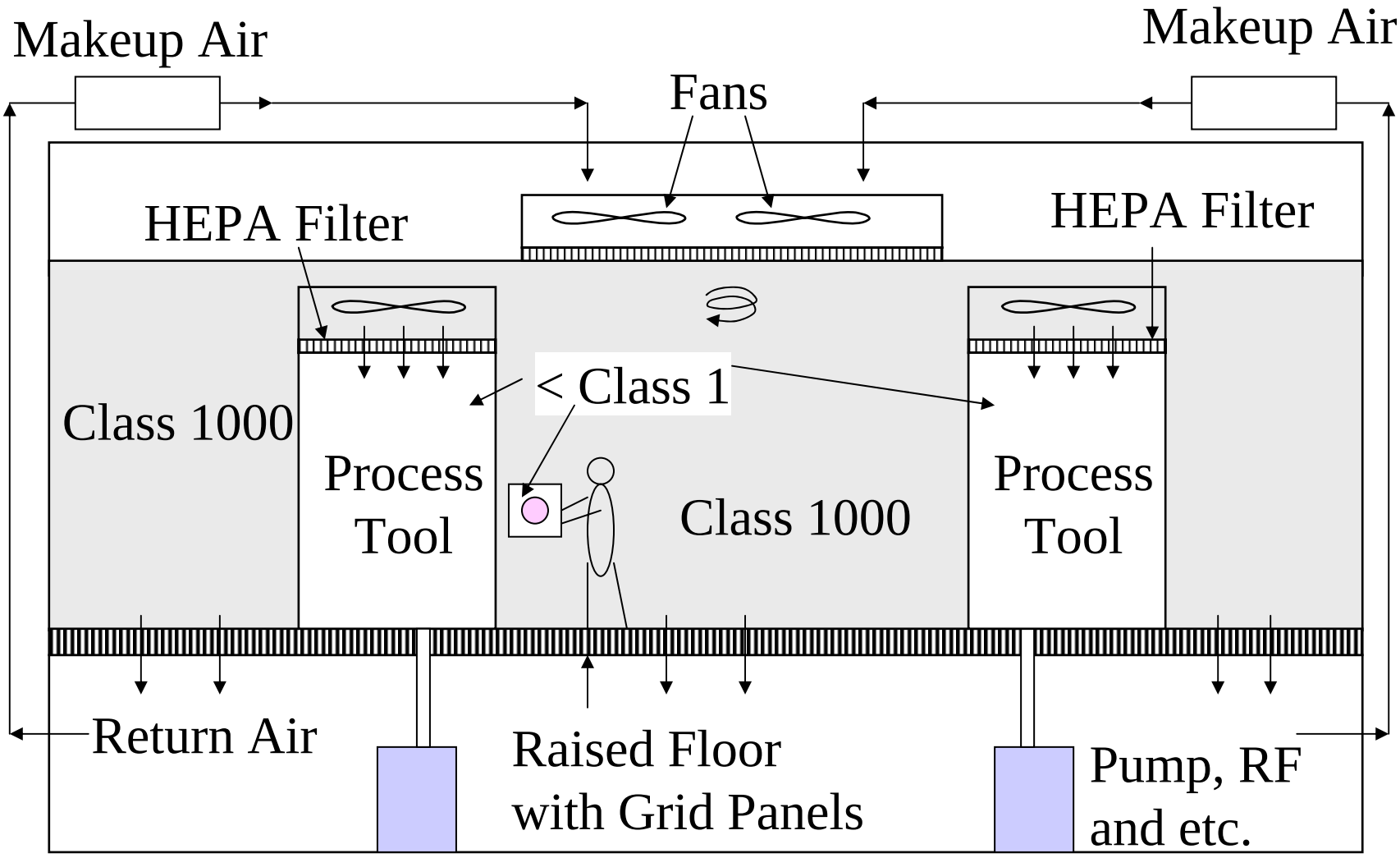
Cleanroom Structure



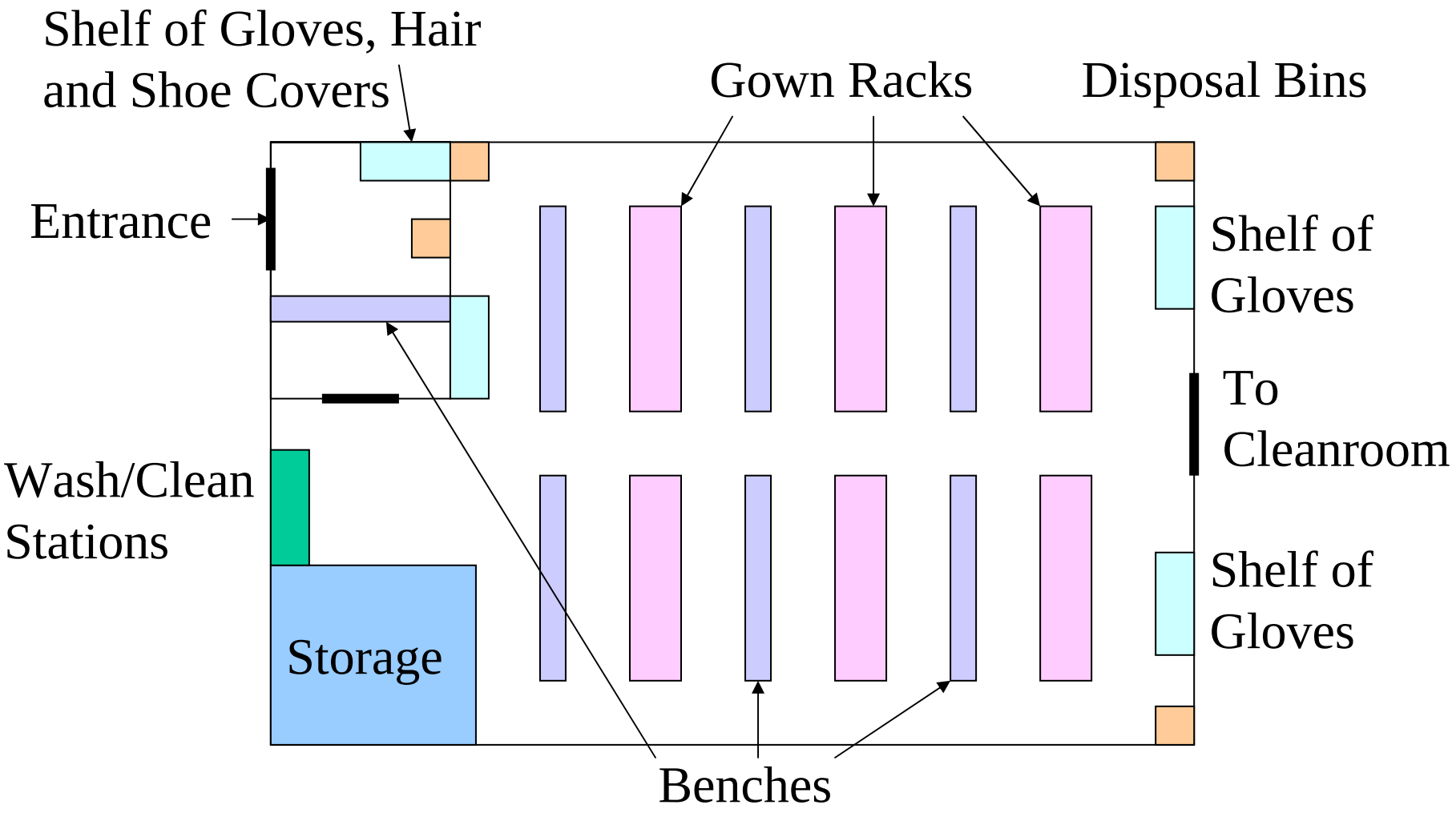
Mini-environment

- Class 1000 cleanroom, lower cost
- Boardroom arrangement, no walls between process and equipment
- Better than class 1 environment around wafers and the process tools
- Automatic wafer transfer between process tools

Mini-Environment Cleanroom



Gowning Area



IC Fabrication Process Module

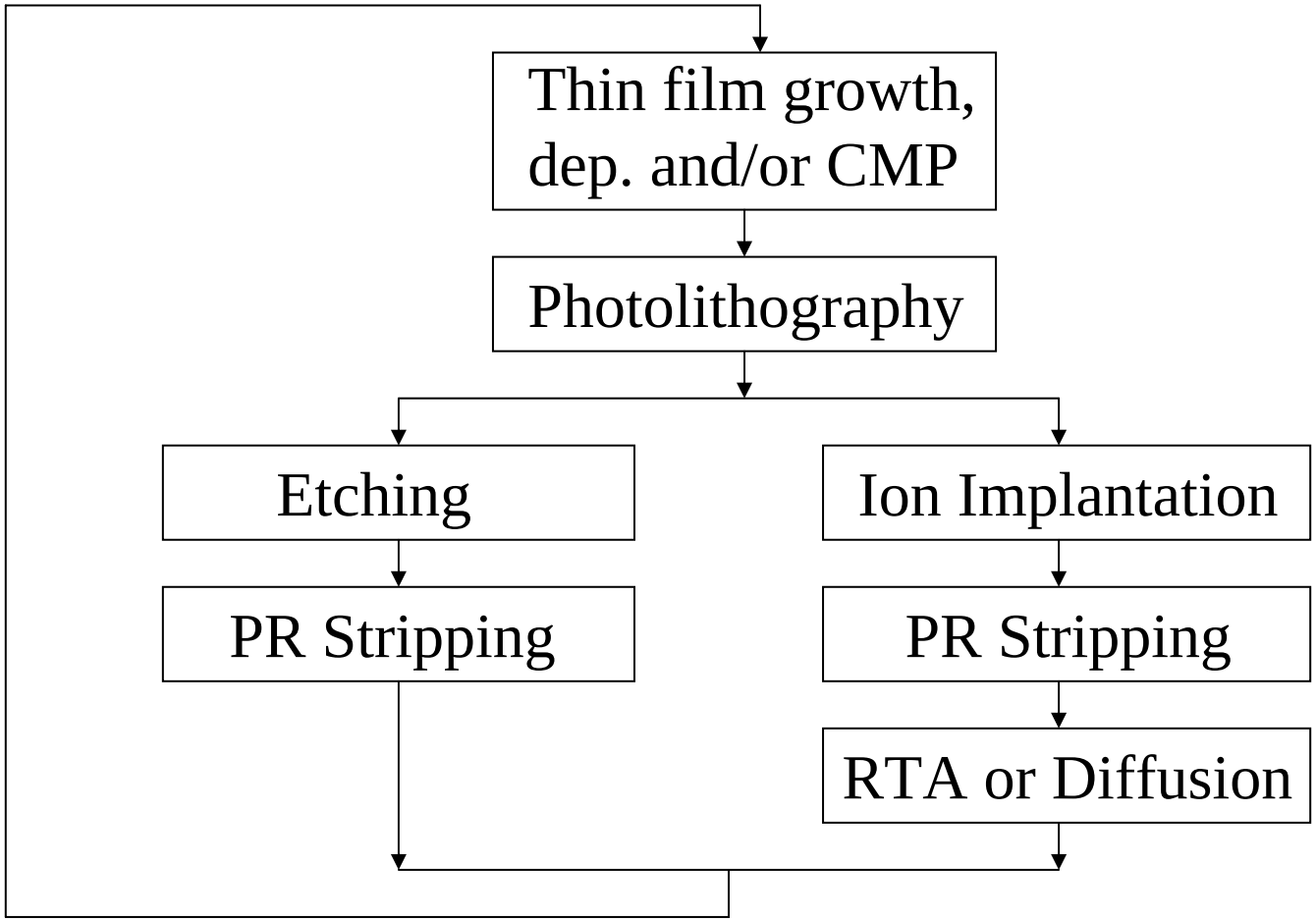
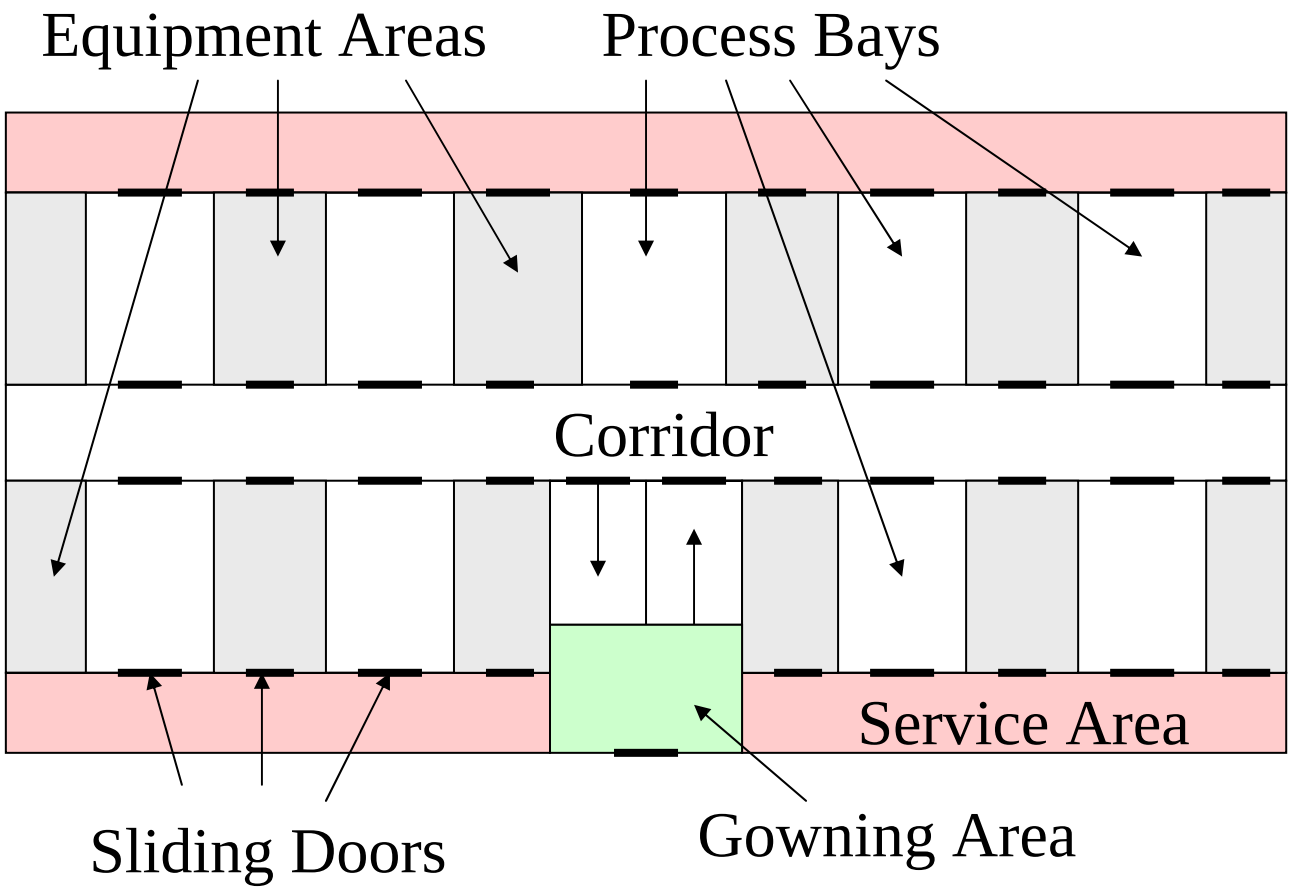
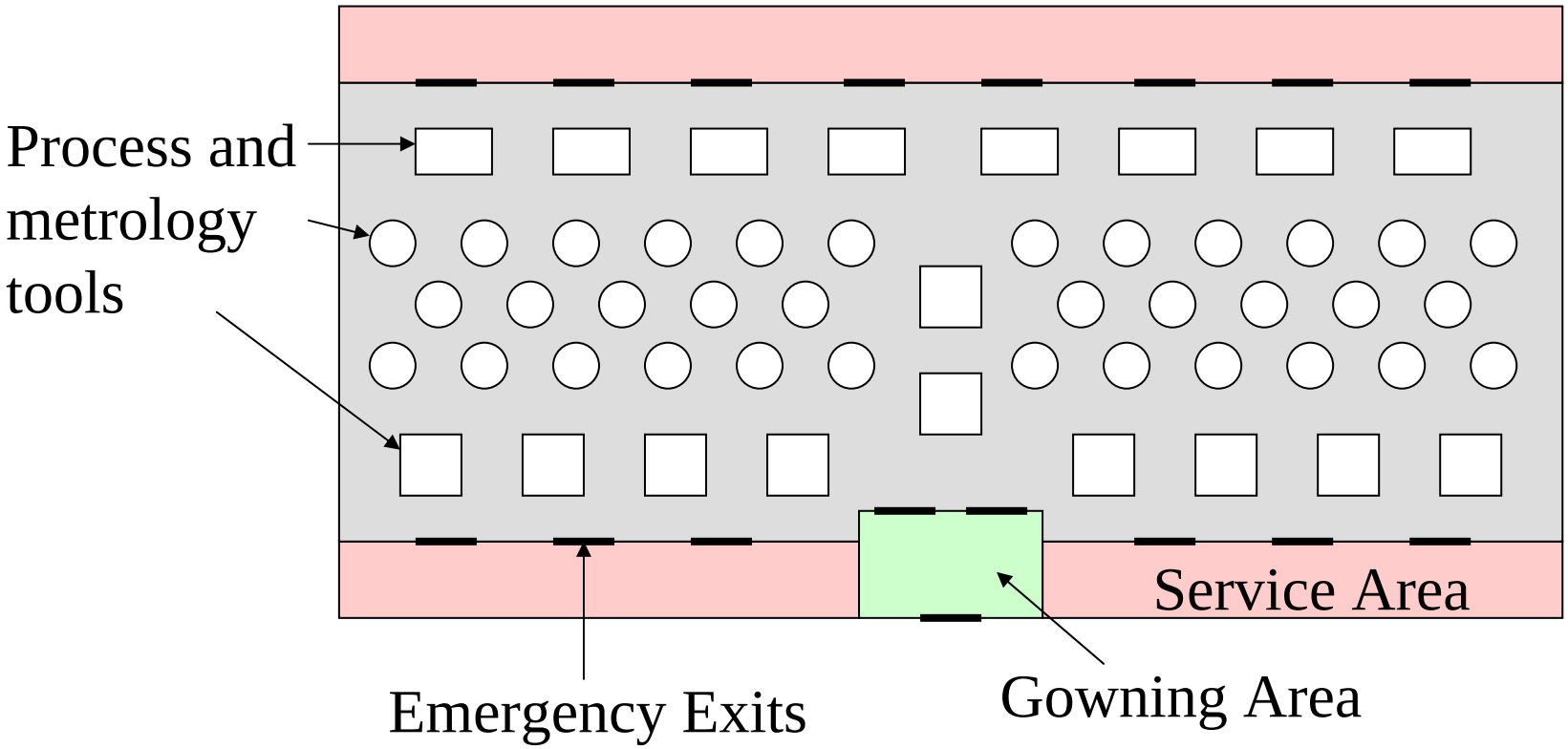


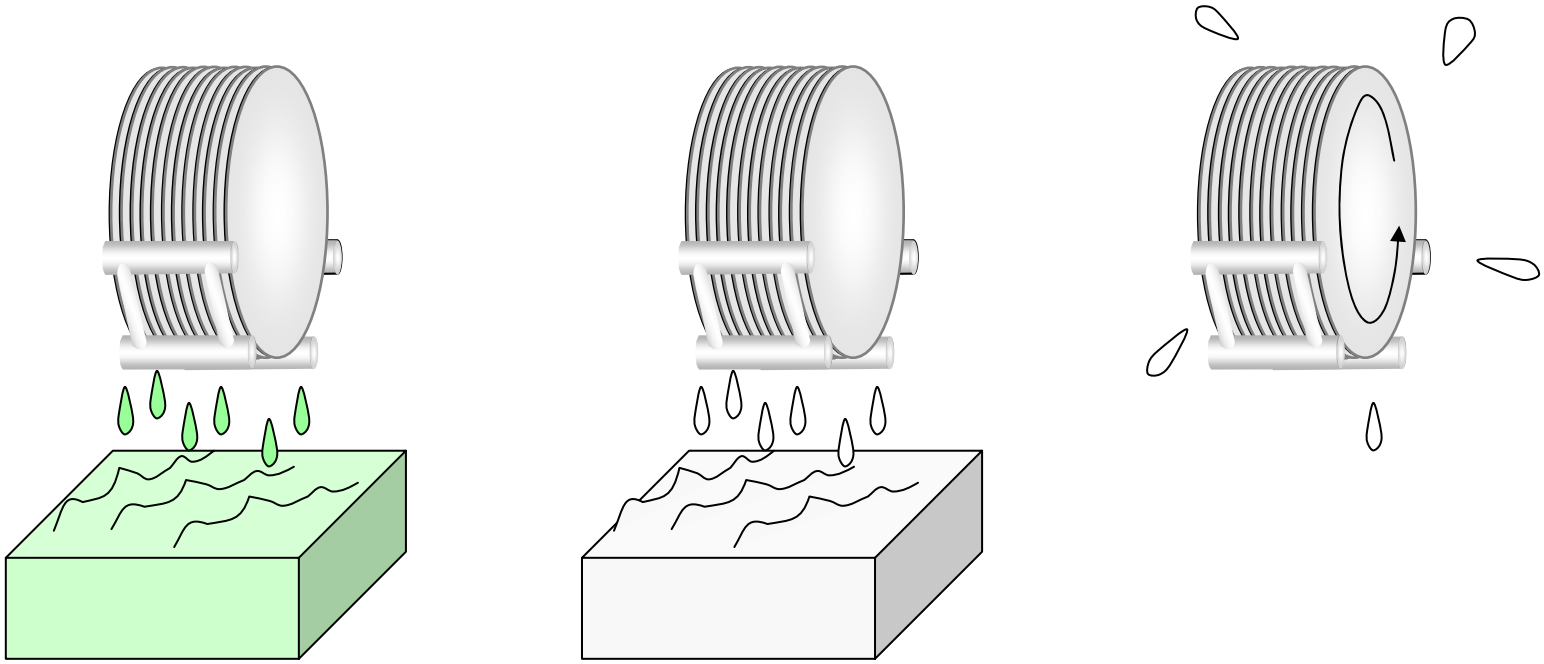
Illustration of Fab Floor



Mini-environment Fab Floor



Wet Processes

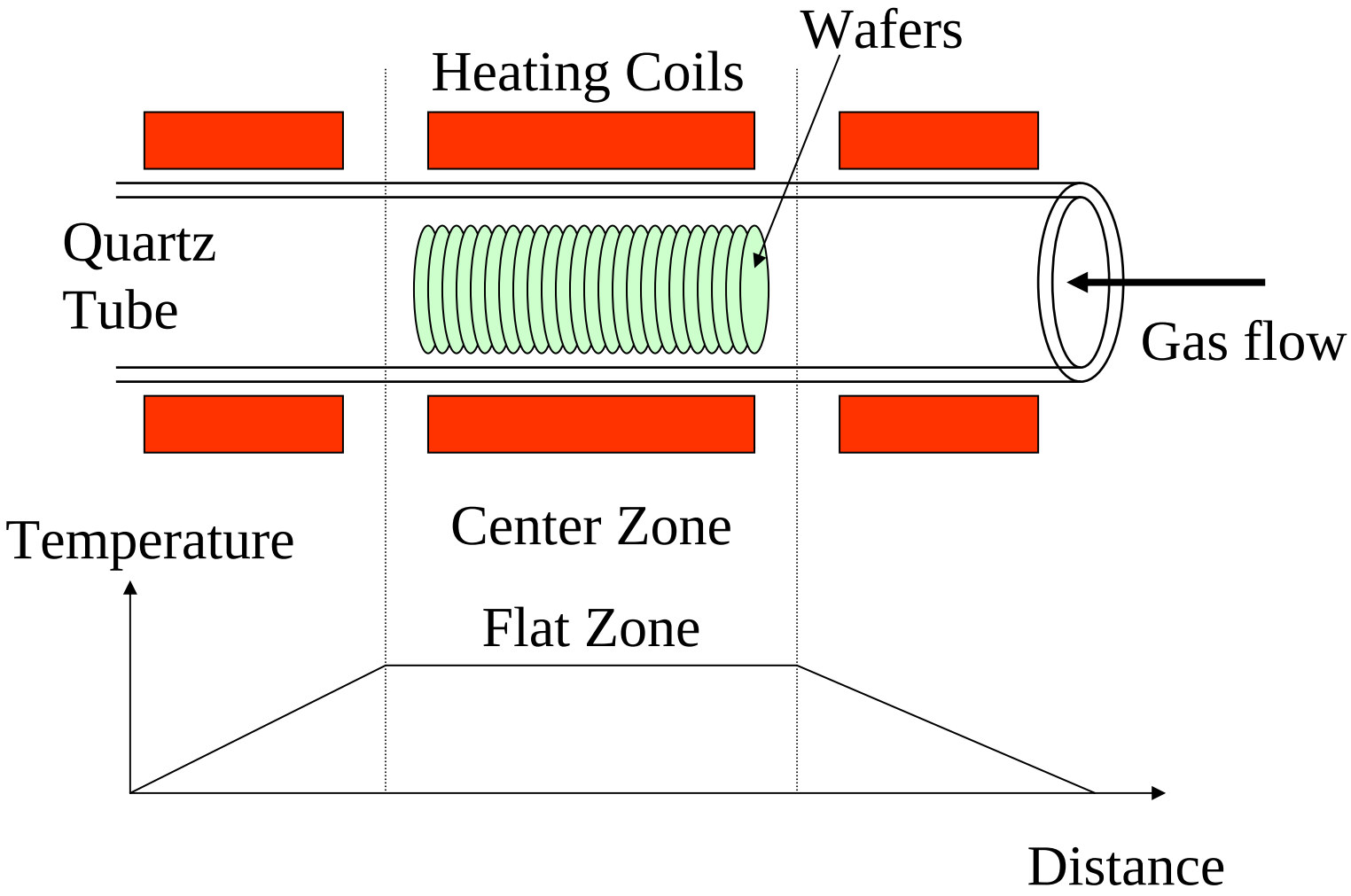


Etch, PR strip, or clean

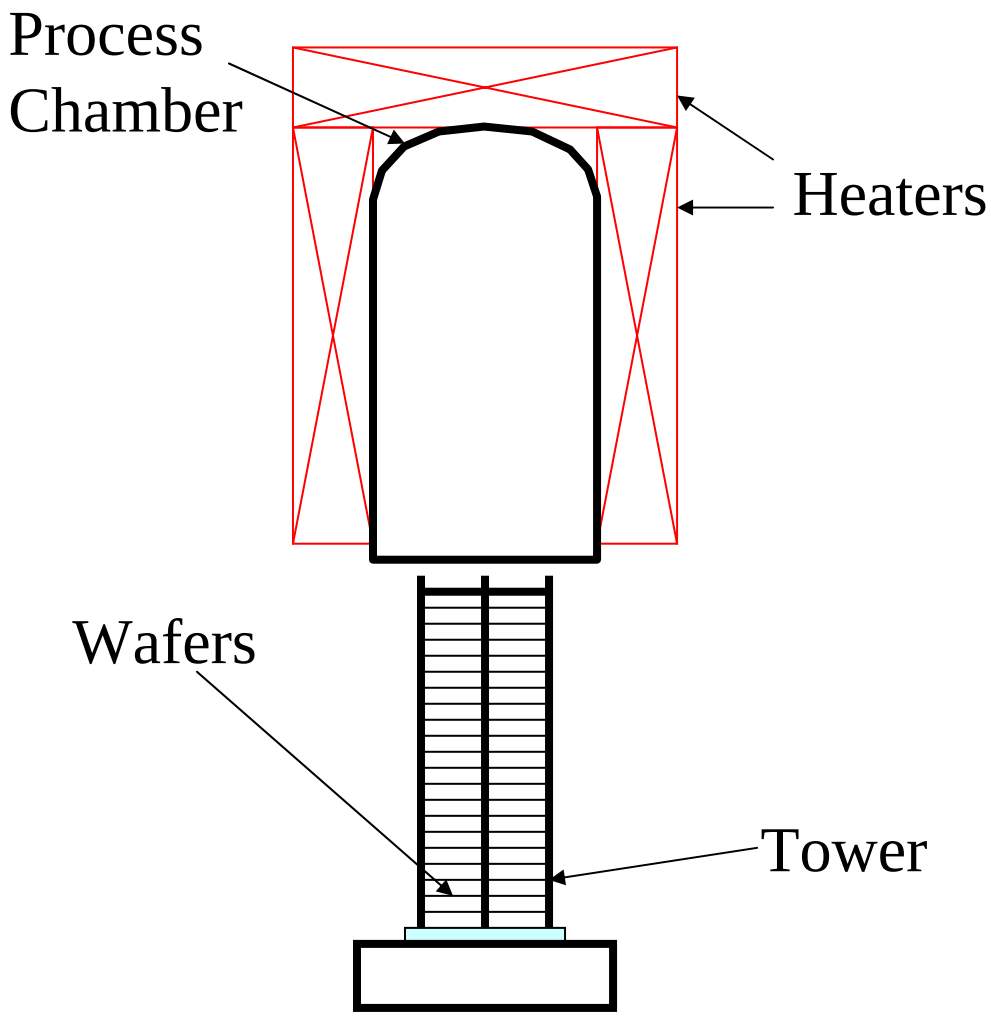
Rinse

Dry

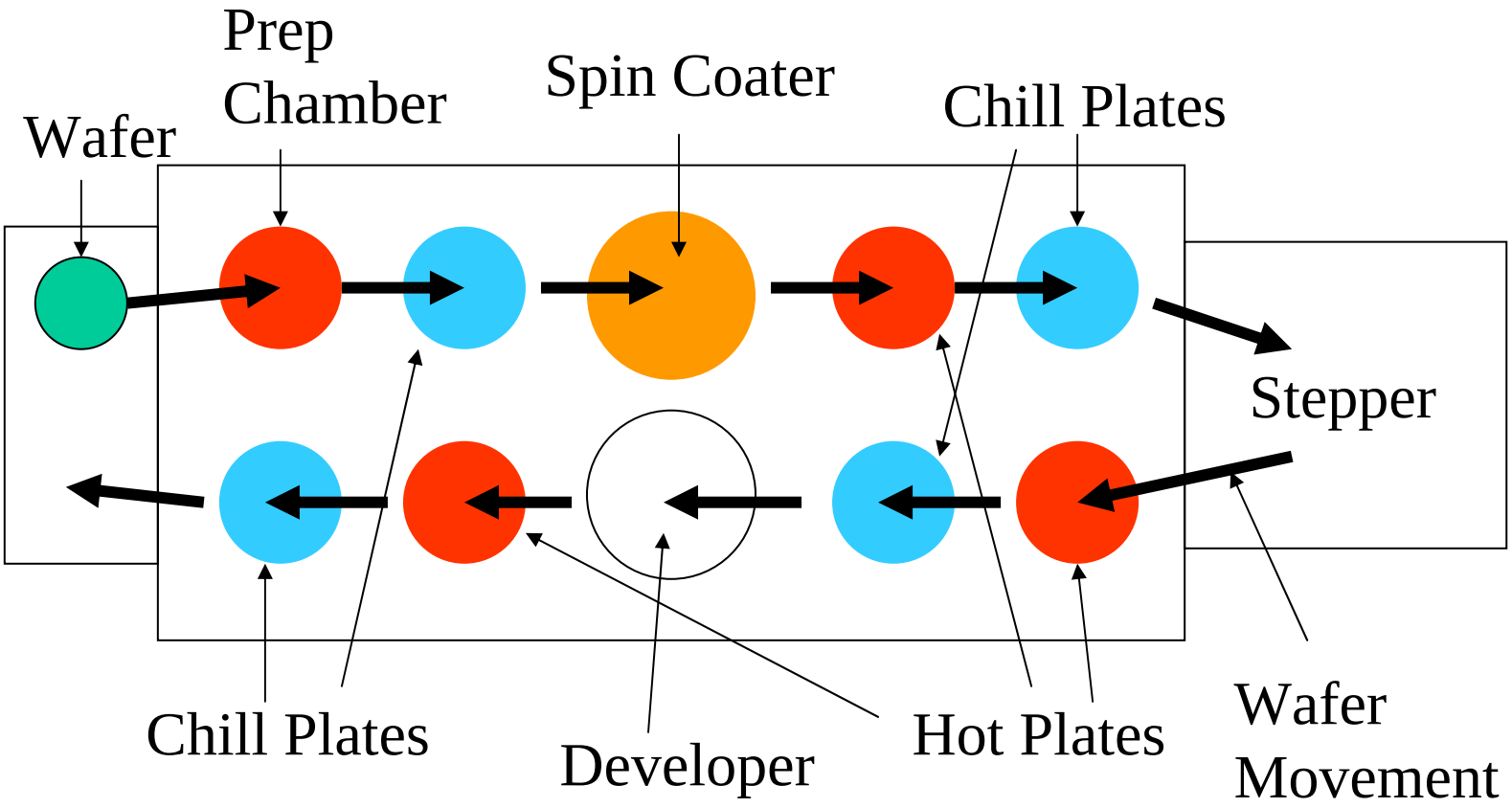
Horizontal Furnace



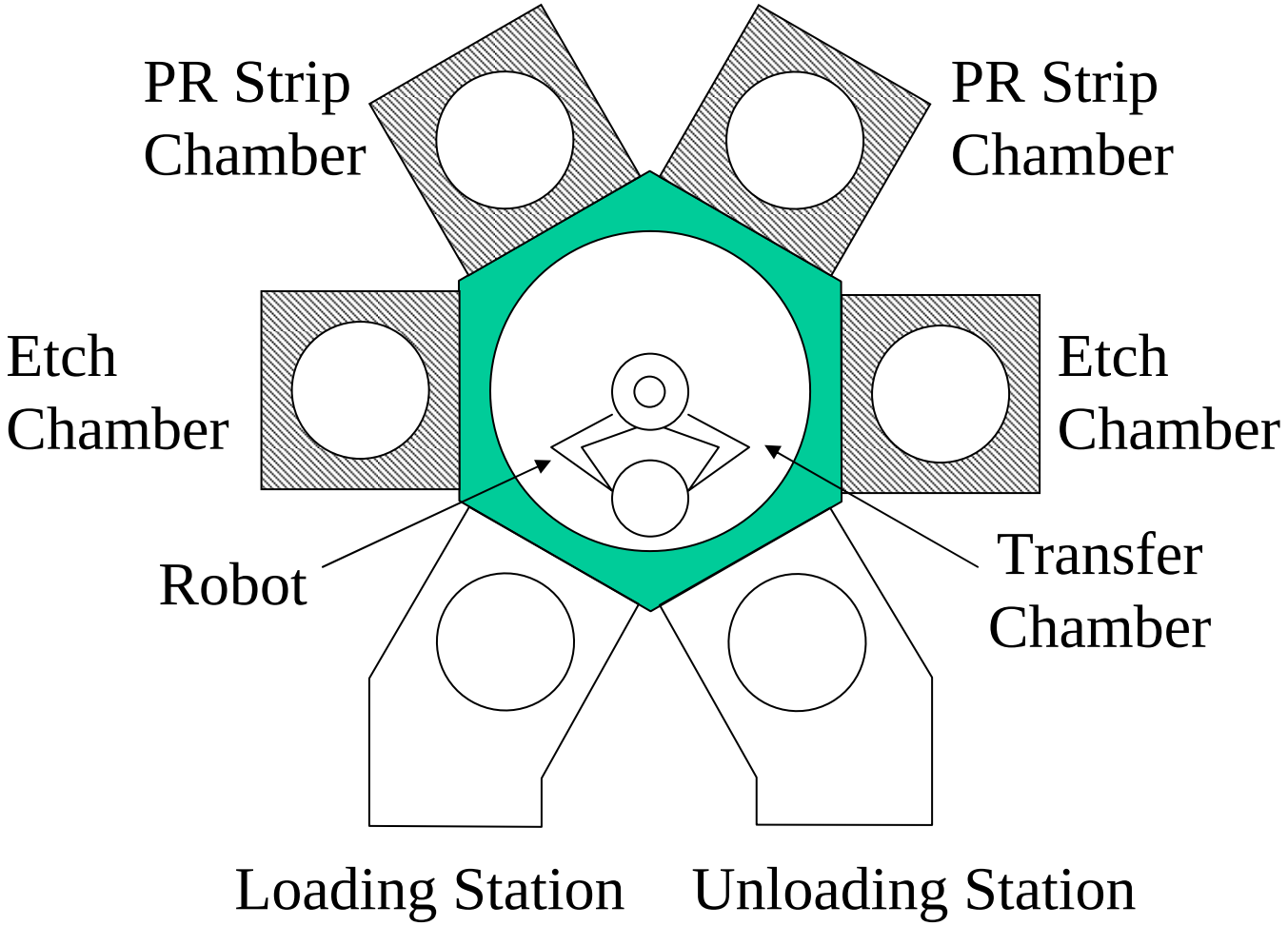
Vertical Furnace



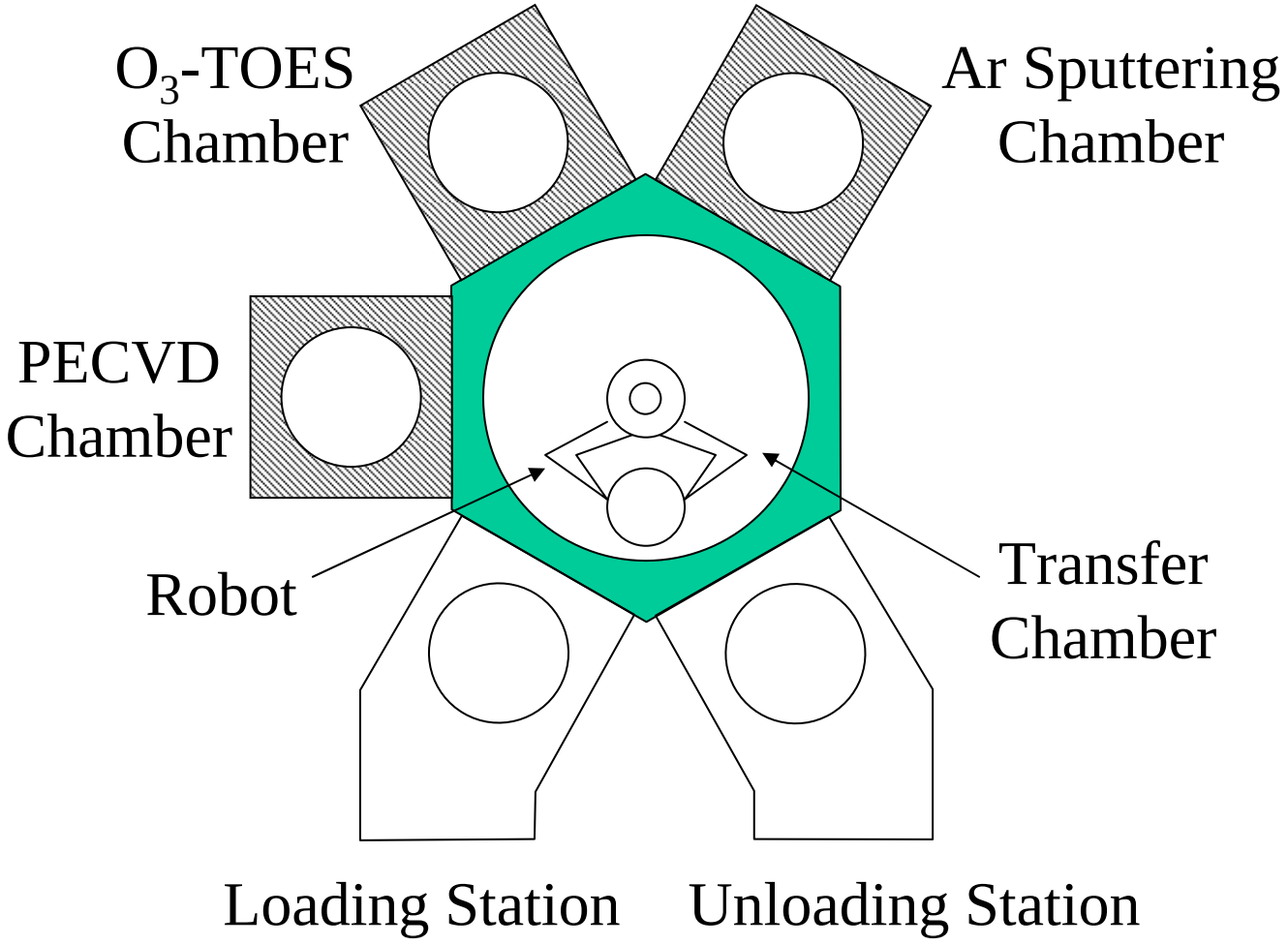
Schematic of a Track Stepper Integrated System



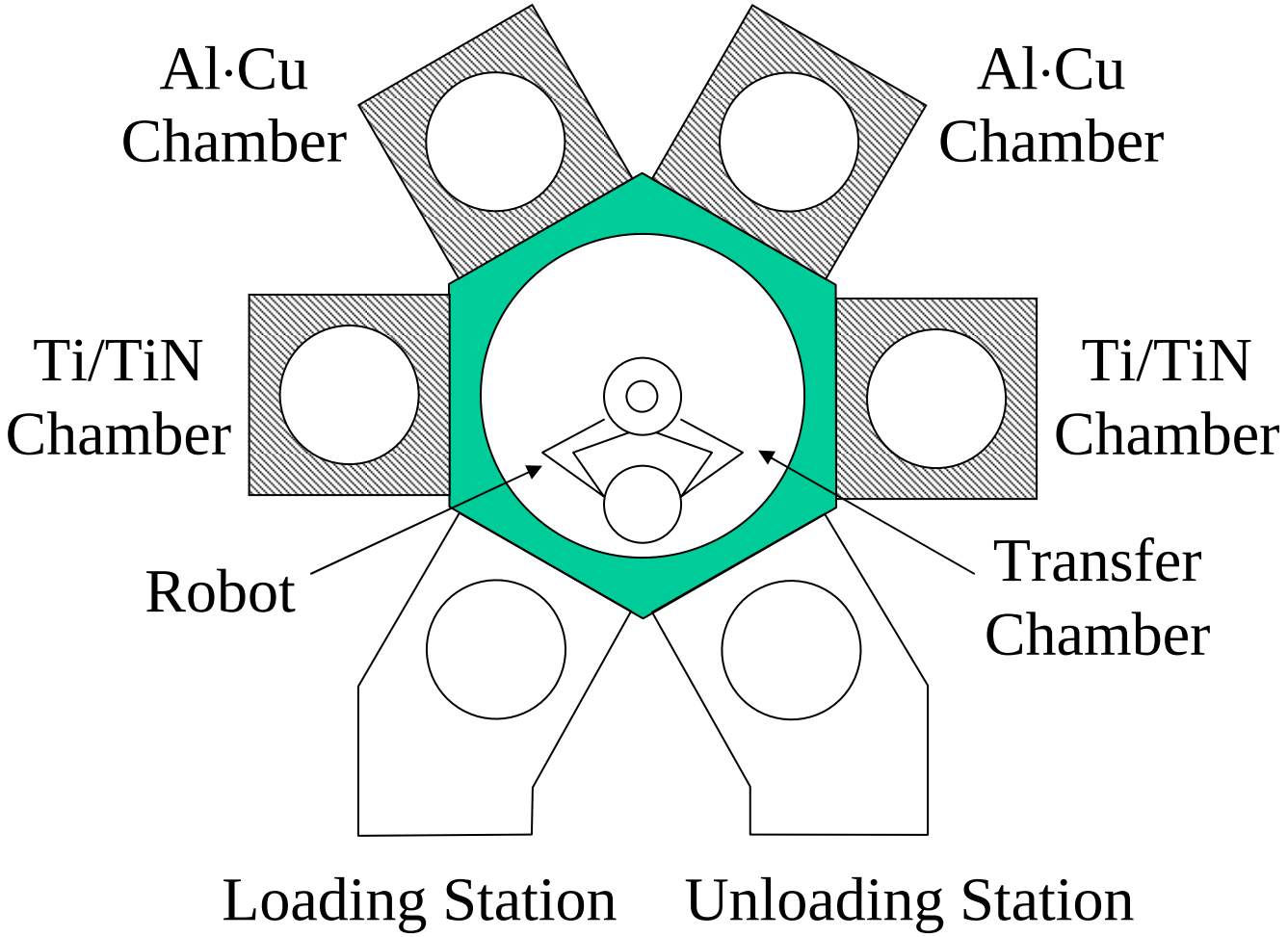
Cluster Tool with Etch and Strip Chambers



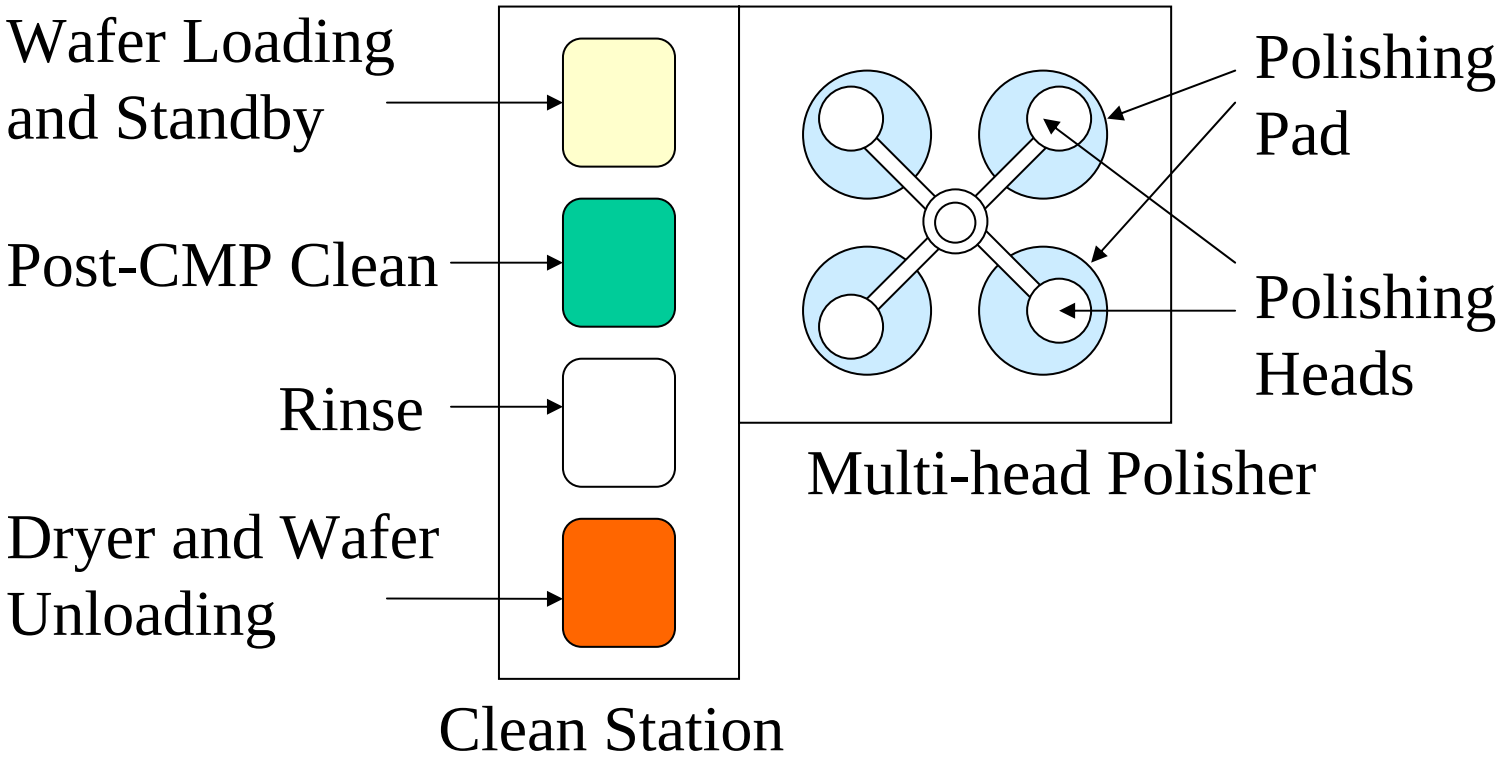
Cluster Tool with Dielectric CVD and Etchback Chambers



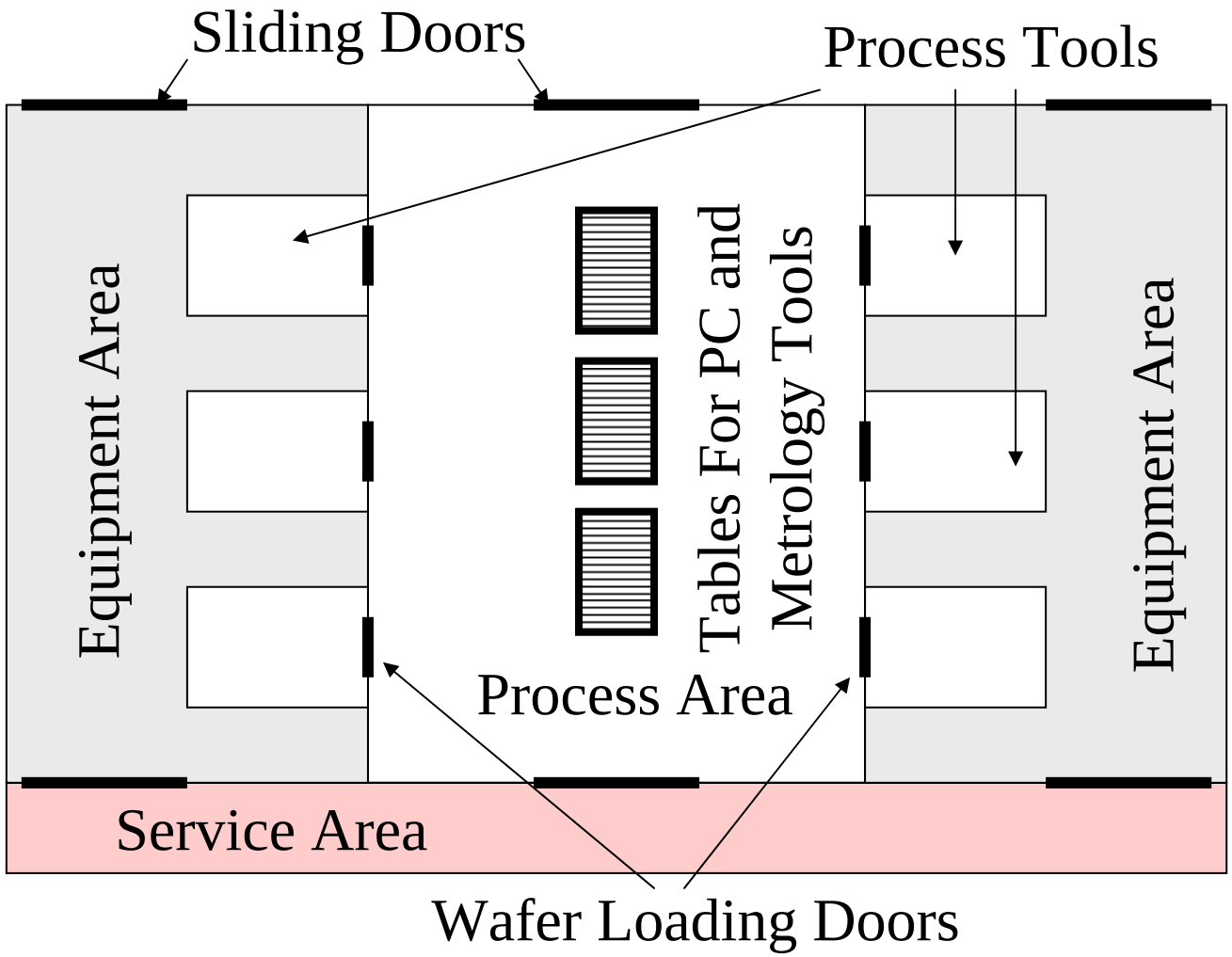
Cluster Tool with PVD Chambers



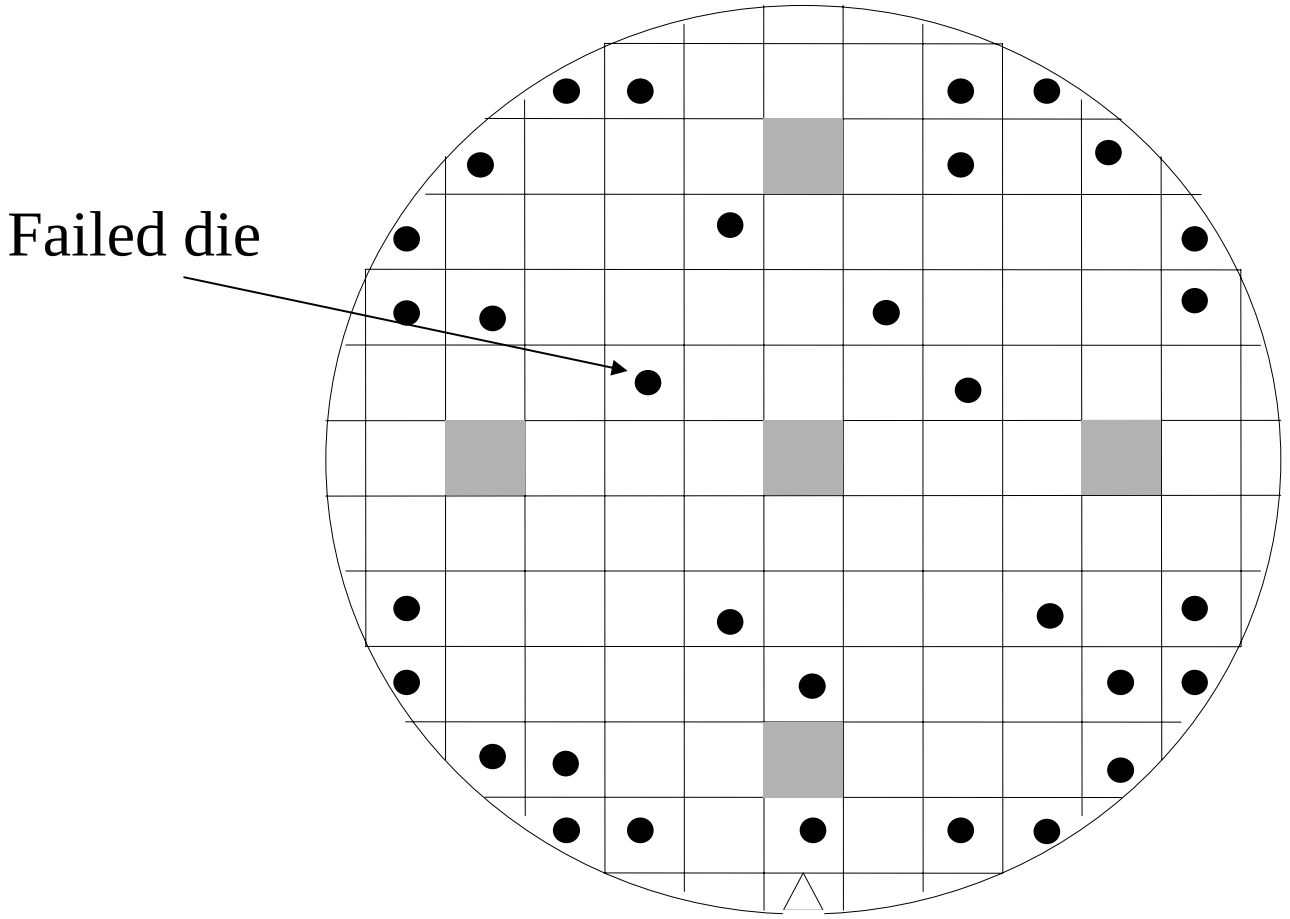
Dry-in Dry-out CMP System



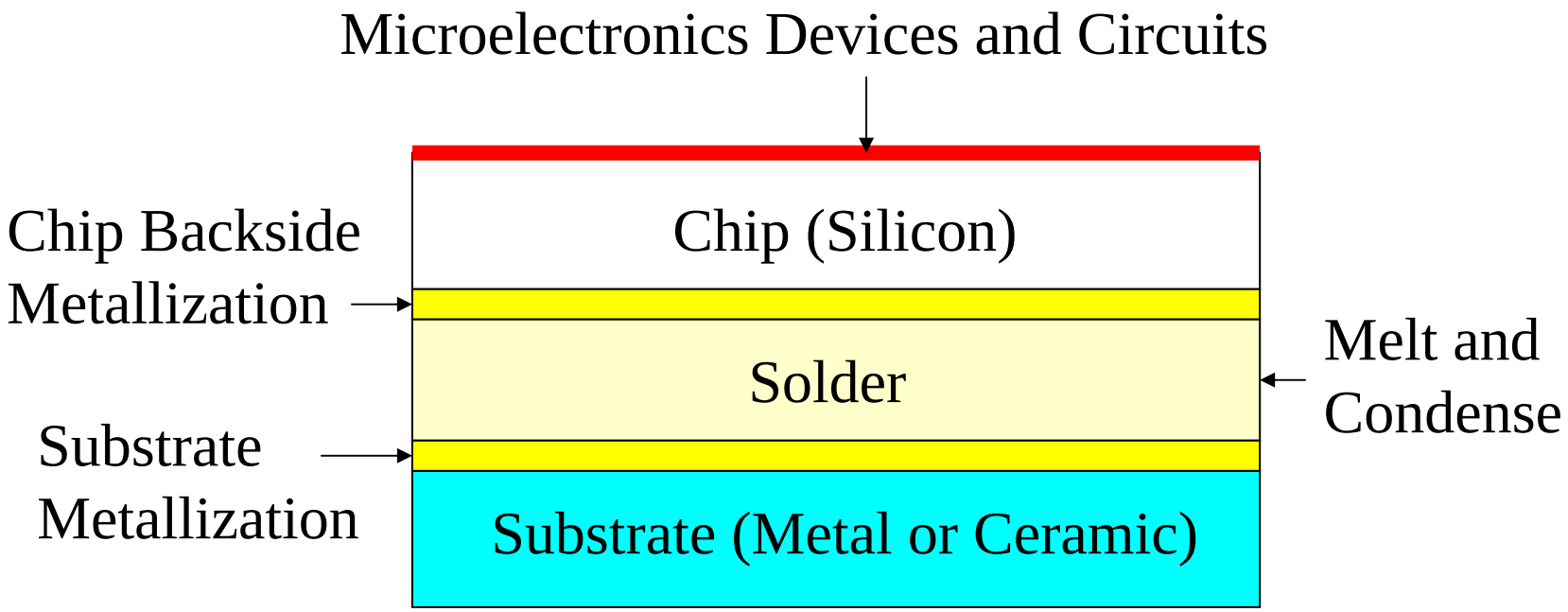
Process Bay and Equipment Areas



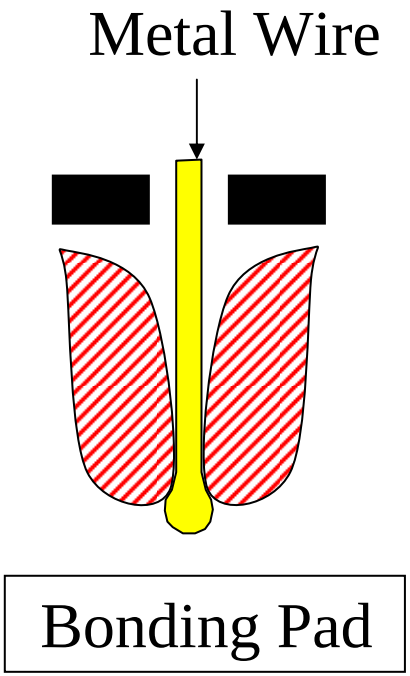
Test Results



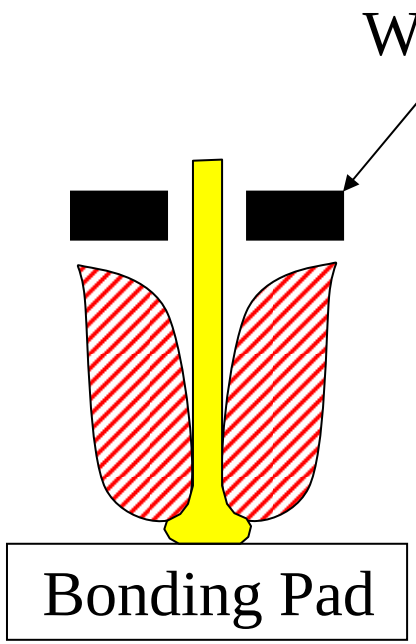
Chip-Bond Structure



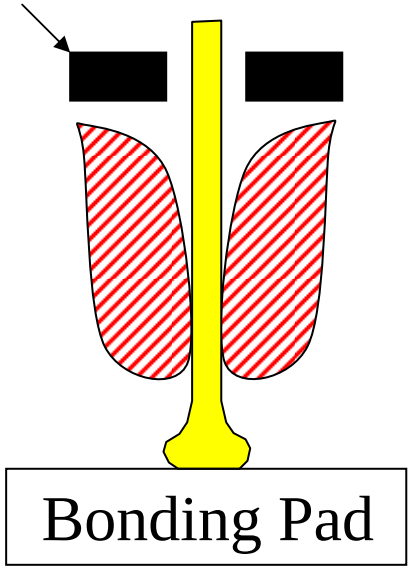
Wire Bonding



Formation of molten metal ball

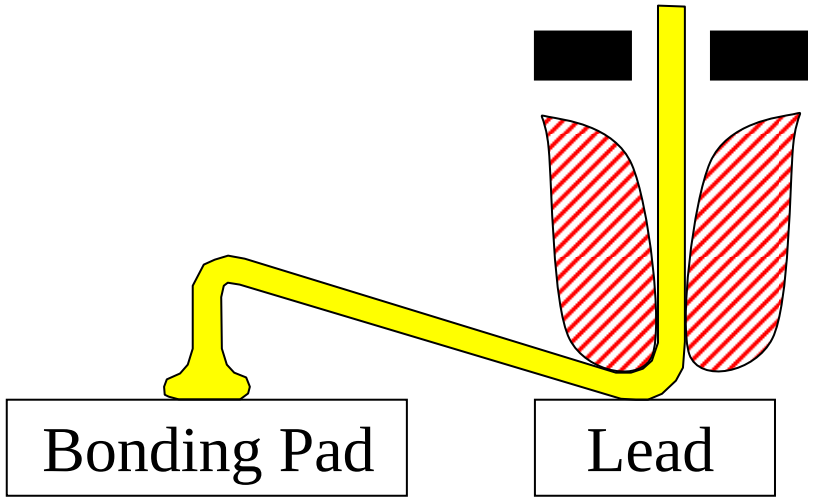


Press to make contact

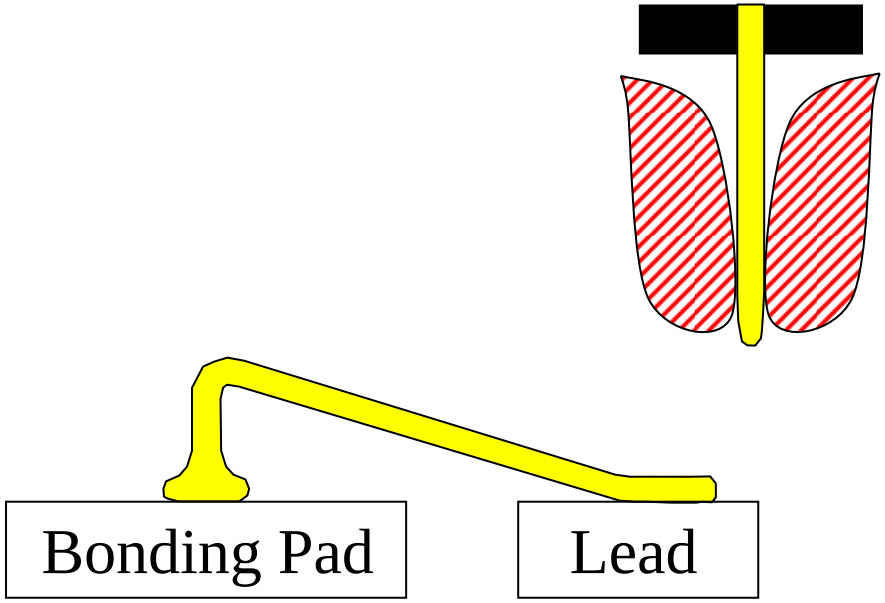


Head retreat

Wire Bonding

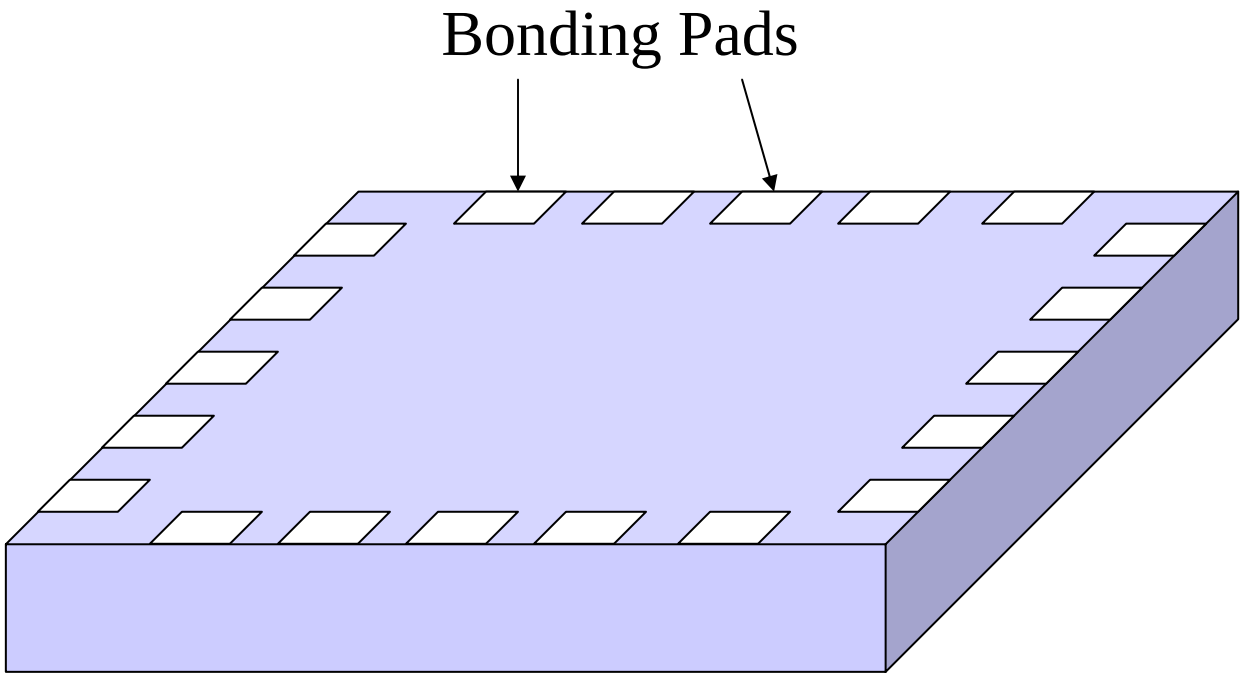


Lead contact with pressure and heat

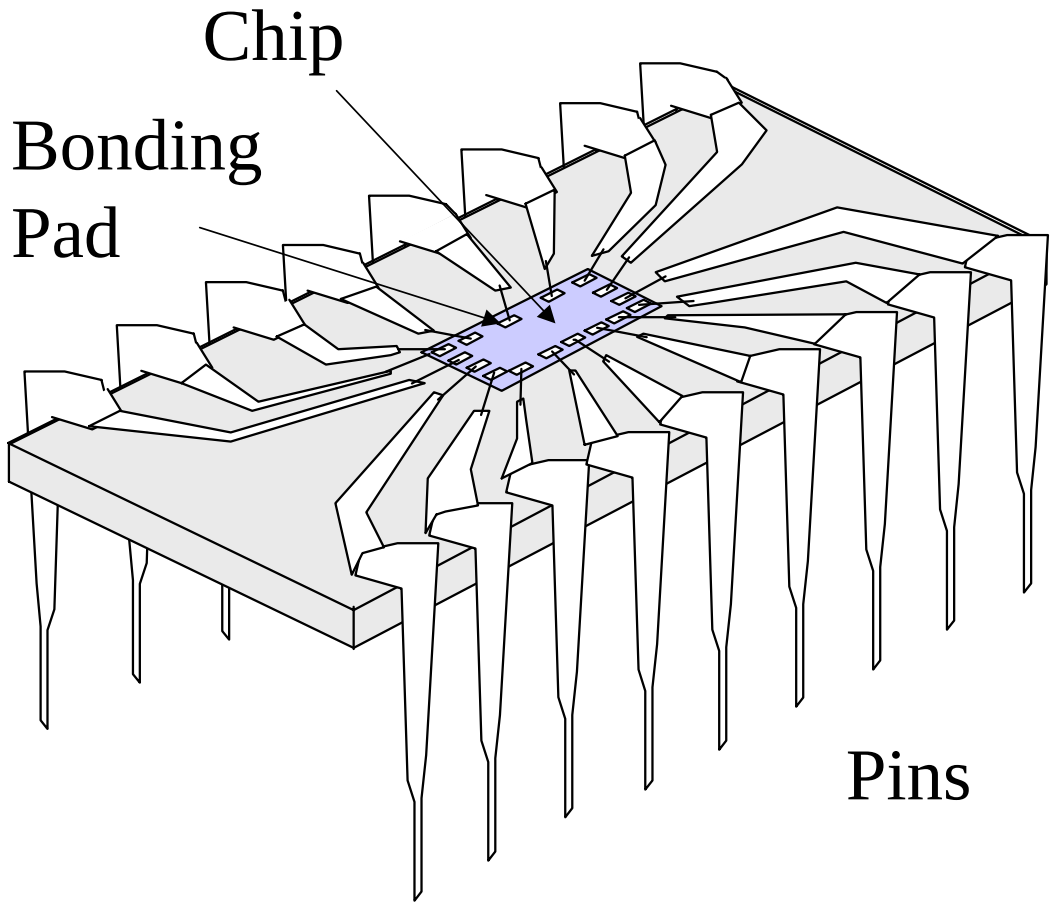


Clamp closed with heat on to break the wire

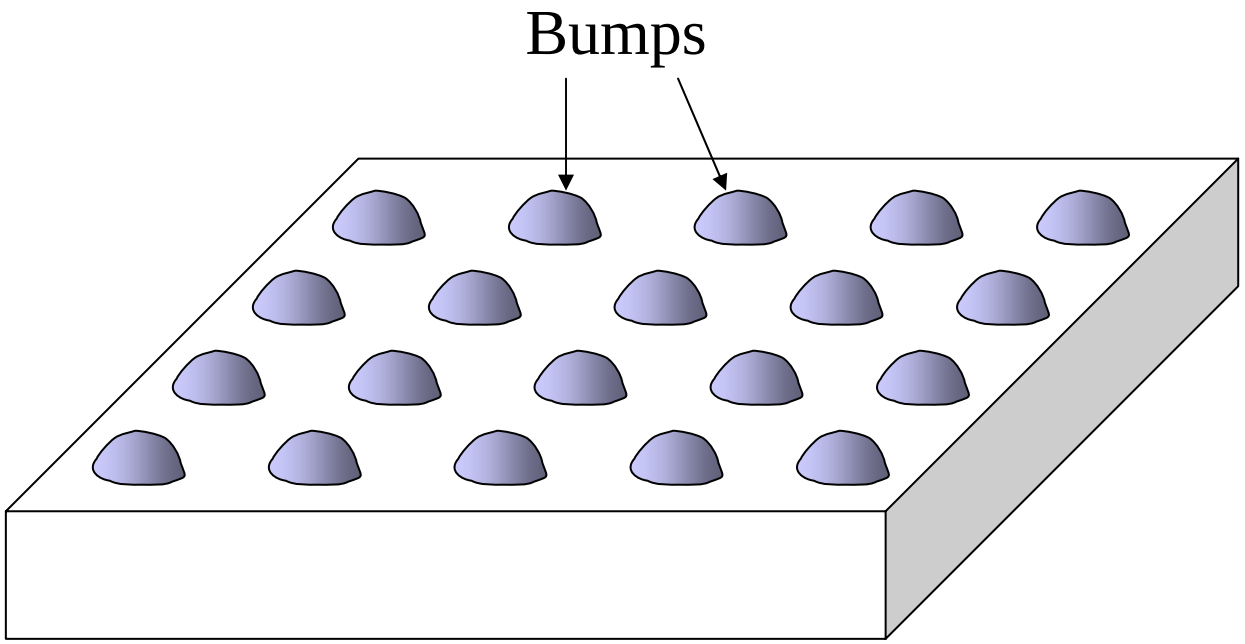
IC Chip with Bonding Pads



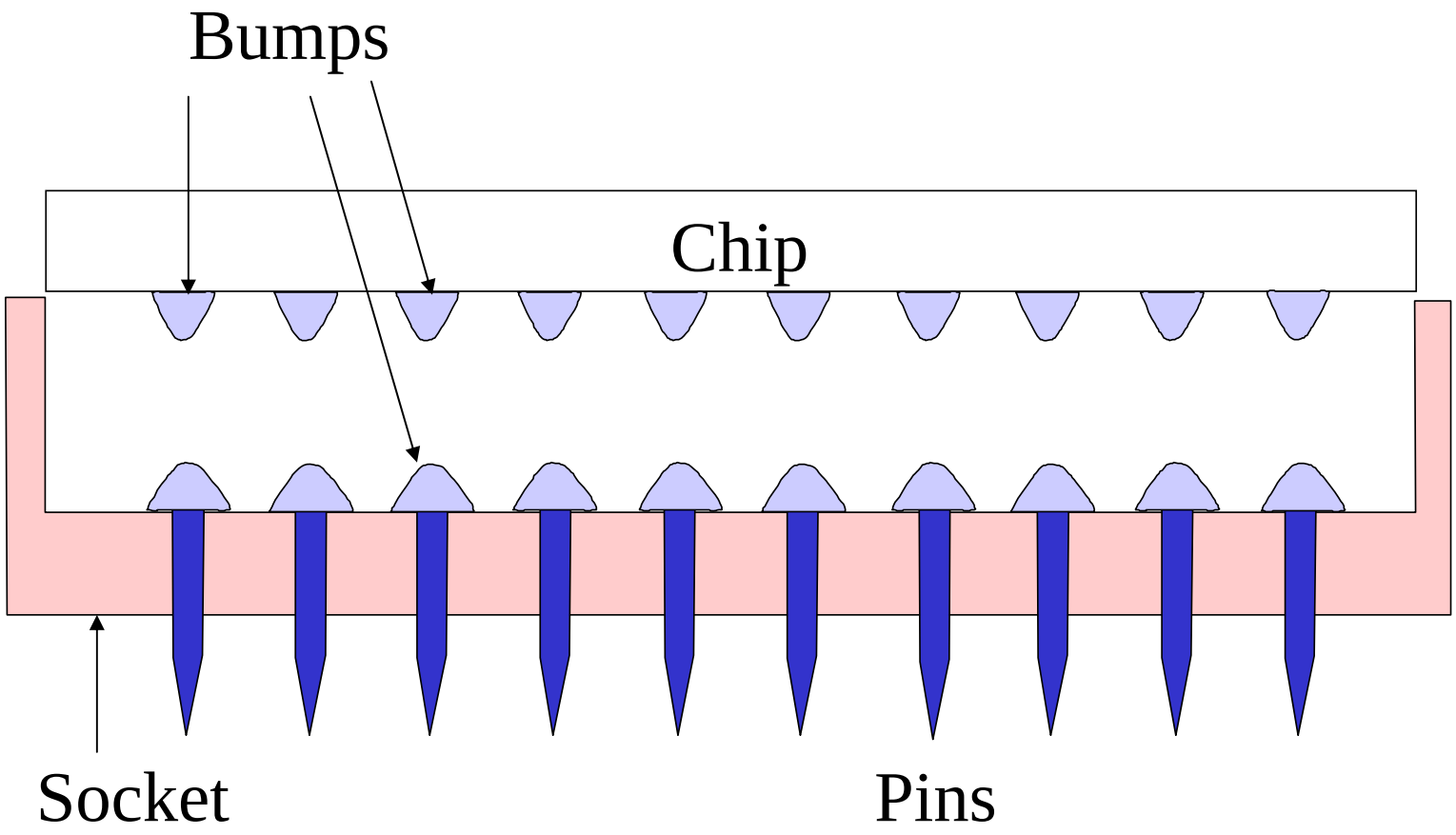
IC Chip Packaging



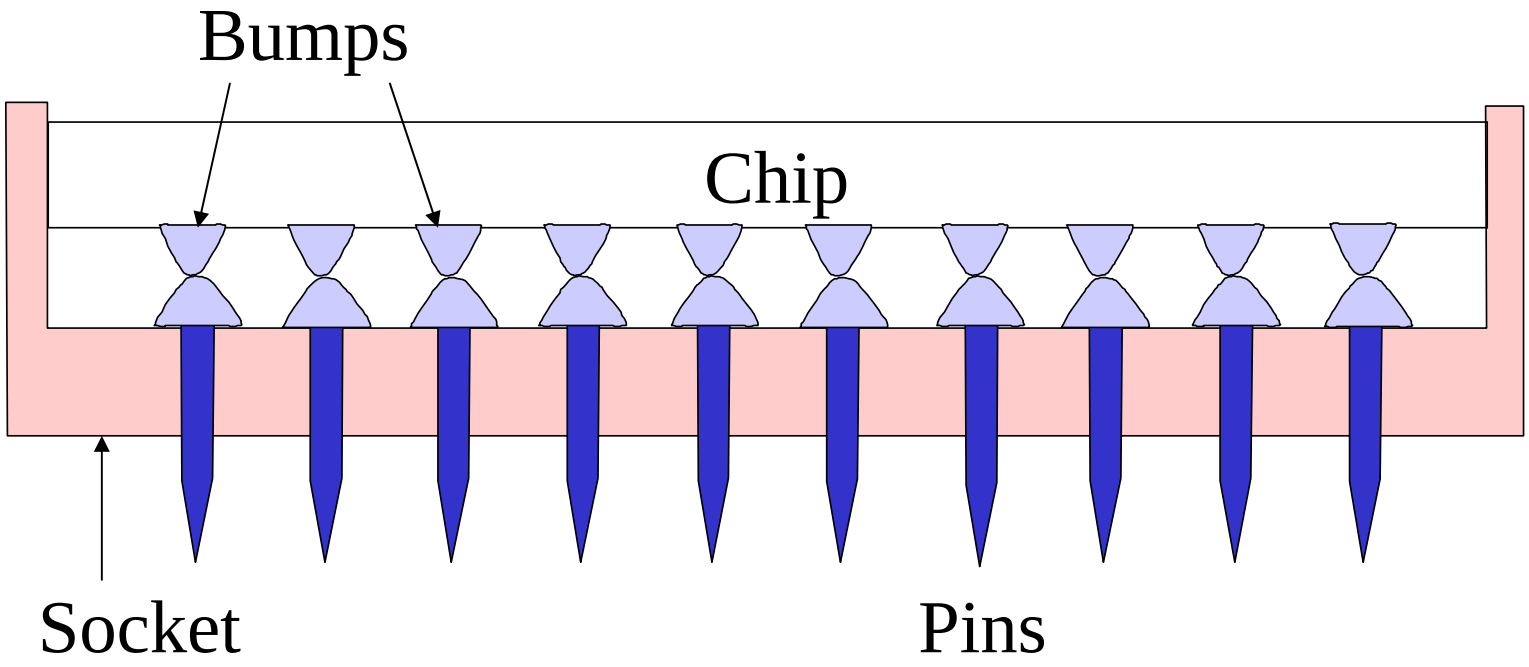
Chip with Bumps



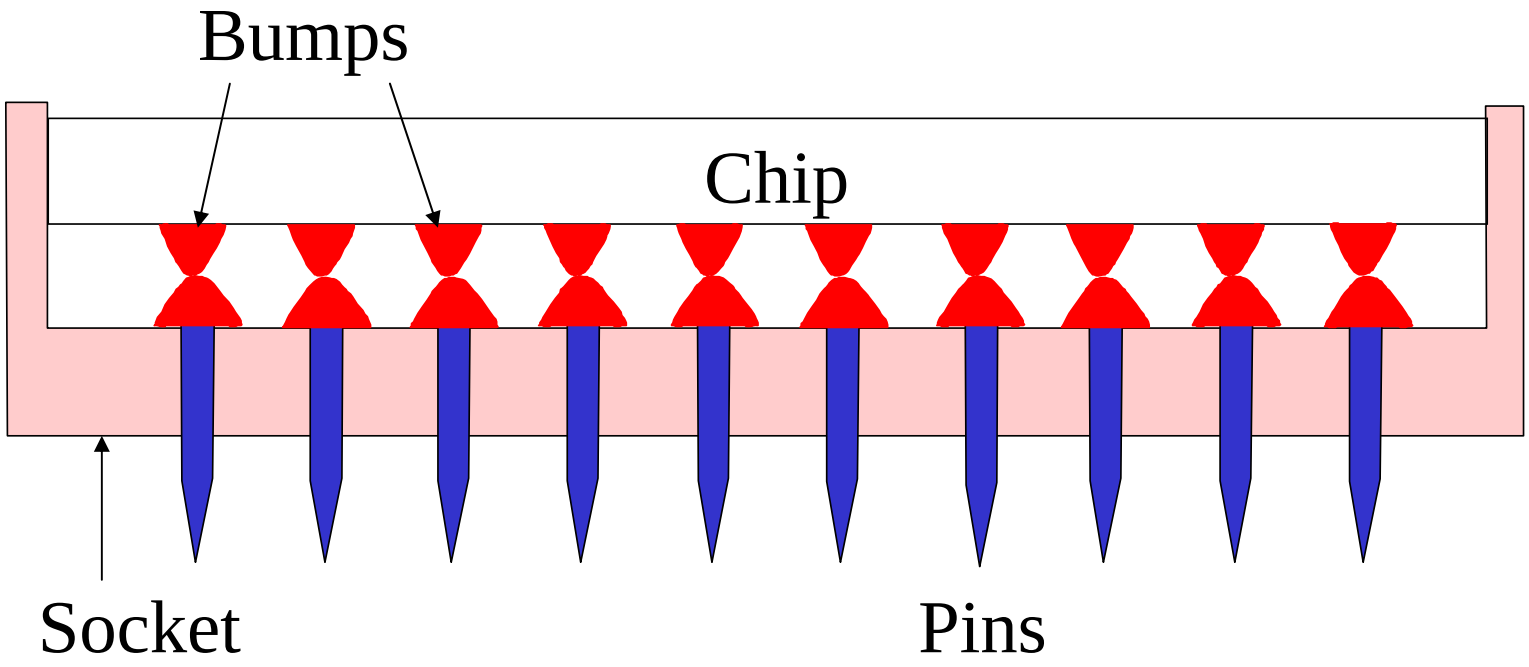
Flip Chip Packaging



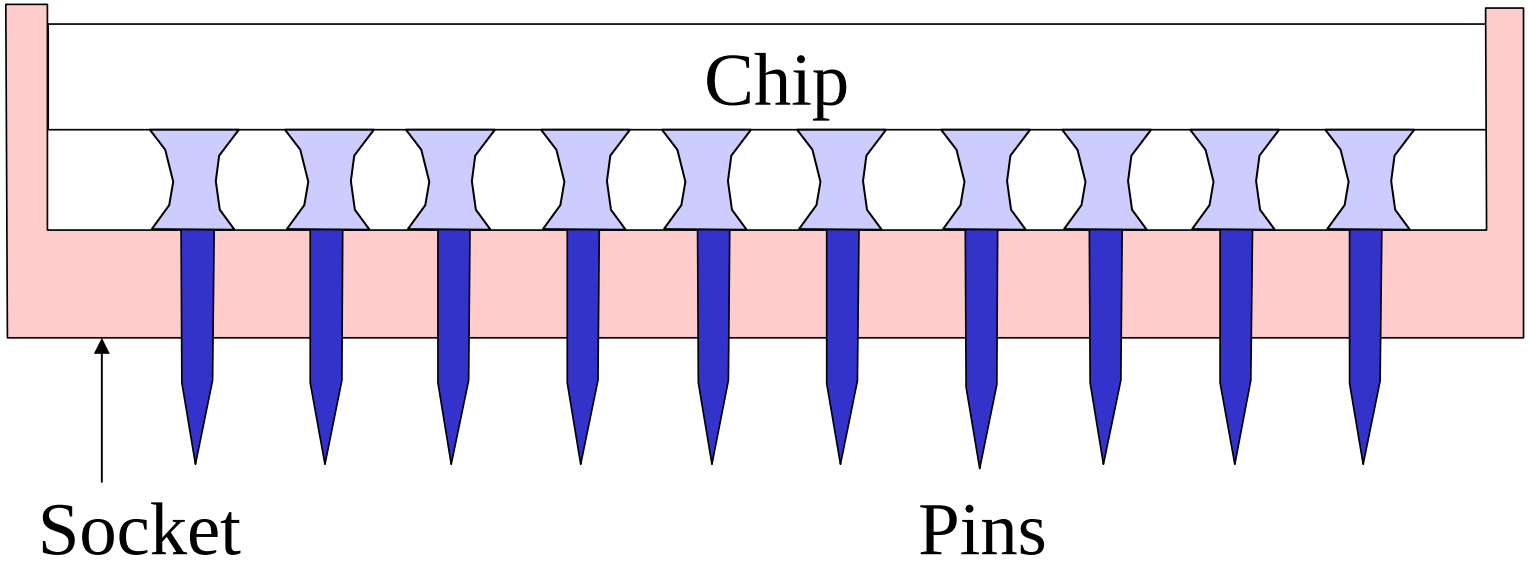
Bump Contact



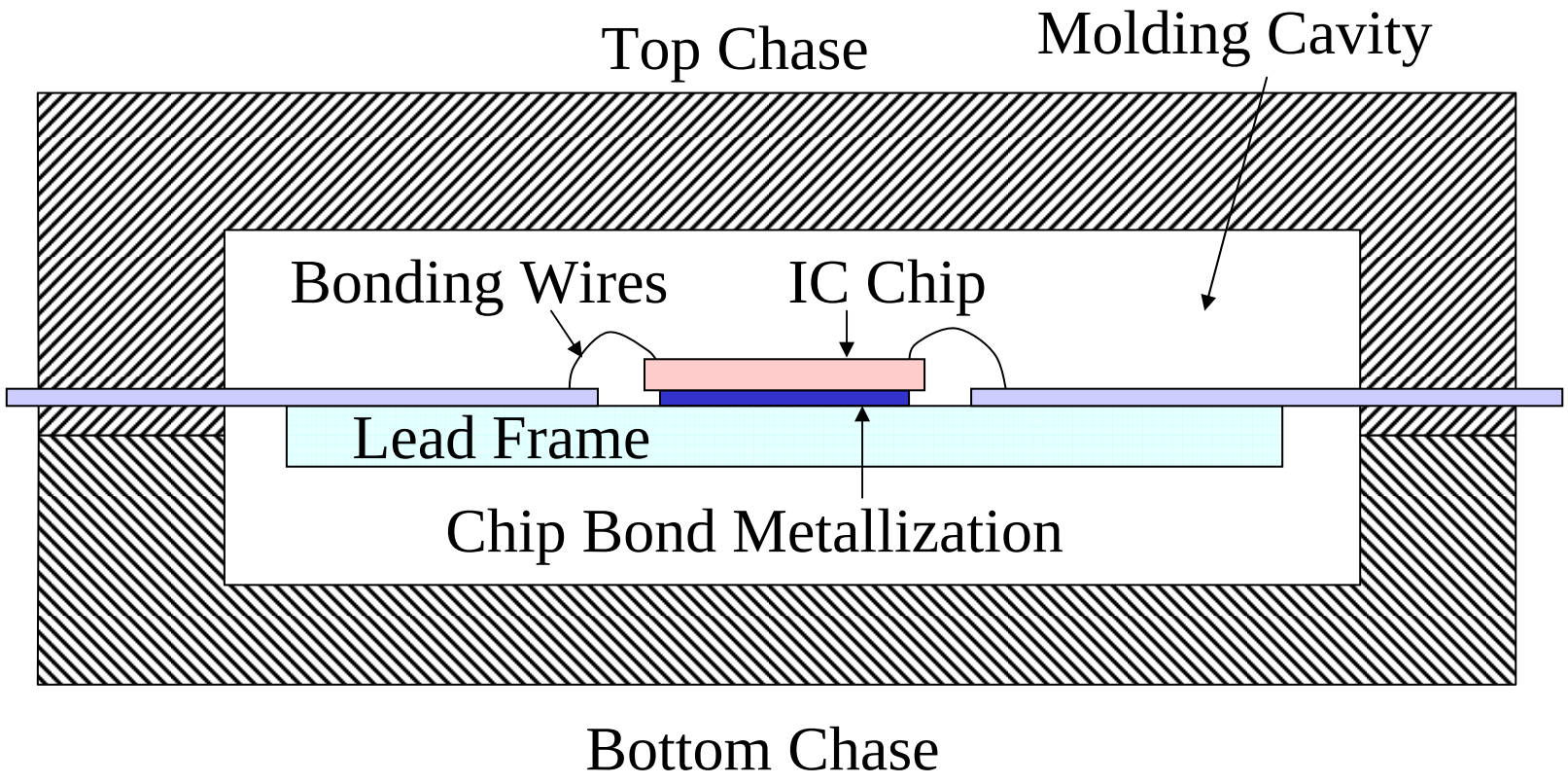
Heating and Bumps Melt



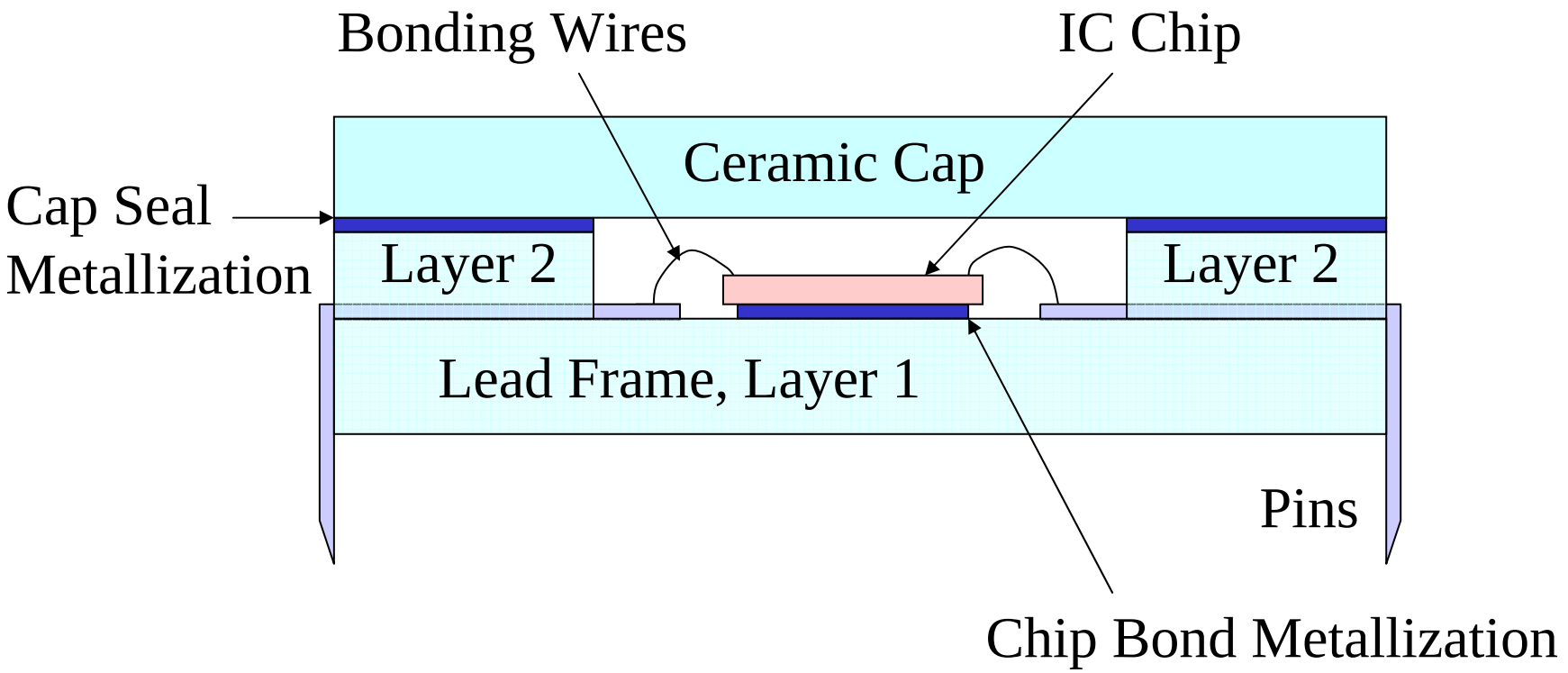
Flip Chip Packaging



Molding Cavity for Plastic Packaging



Ceramic Seal



Summary

- Overall yield
- Yield determines losing money or making profit
- Cleanroom and cleanroom protocols
- Process bays
- Process, equipment, and facility areas
- Die test, wafer thinning, die separation, chip packaging, and final test