Medium energy ion scattering studies of high-κ dielectric gate stacks

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The reduction of the effective gate oxide thickness has become a challenge for the continuous drive to higher packing density and performance of devices. One way to overcome this problem is the replacement of SiO$_2$ by a material with a larger permittivity, a high-κ dielectric. Additional advantages can be gained by building faster electronics based on higher carrier mobility materials, such as Ge and III-V substrates. Problems relating to the stability of such oxides need to be addressed if high-κ materials are to be incorporated into conventional device processing. Along with high permittivity, alternative gate dielectrics must satisfy other strict demands, including an appropriately large band gap with sufficient conduction and valence band offsets (with respect to Si), proper morphology, high interface quality (low electron trap density and small roughness), and high chemical stability with MOSFET channel and gate electrode materials. The latter requirement restricts the high-κ candidates to a narrow group of metal oxides and silicates, such as ZrO$_2$ and HfO$_2$.\(^1\) Though stable with respect to decomposition via solid-state reactions, at elevated temperatures these oxides can still decay with desorption of gaseous SiO (process 1a) accompanied by metal silicide formation (1b):

\[
\begin{align*}
\text{MO}_2(s) + 2\text{Si}(s) & \rightarrow \text{M}(s) + 2\text{SiO}(g) \\
\text{M}(s) + 2\text{Si}(s) & \rightarrow \text{MSi}_2,
\end{align*}
\]

where M = \{Zr, Hf\}. In practice, it is usually not possible to avoid a very thin interfacial SiO$_2$ layer between the high-κ material and the substrate. This influences the interfacial electrical properties and dielectric stack thermal stability; therefore a precise control of the interfacial oxide is essential during processing. One way to obtain information on the buried interface thickness is by cross-sectional transmission electron microscopy (TEM). This method requires careful sample preparation, and does not always provide a satisfactory contrast to discriminate between the stack components. Medium energy ion scattering (MEIS) has proven to be an appealing alternative. MEIS can be thought of as a low energy, high resolution version of conventional RBS. This presentation illustrates the application of MEIS to the analysis of...
interface composition and thickness, and its evolution during growth and post-processing for high-k stacks fabricated on Si and GaAs substrates.

In MEIS, the scattered-ion intensities (typically 50 – 200 keV H+ or He+) are measured as a function of the scattering angle and energy. The energies of the backscattered ions are related to their incident energy via a kinematic factor, which is a function of a target atom mass and scattering angle. While traversing the solid, the ions lose energy to electron excitations. The energy loss is proportional to the traveled distance, and therefore the layer thickness and depth can be determined from the peak width and position, respectively. Knowledge of the scattering cross sections allows a quantitative compositional analysis.

In the first example, several ZrO2 samples with a thickness of 3.5 – 20 nm were grown by ALD on 1-nm thick wet SiO2. Fig. 1 shows a representative set of MEIS spectra for the as-fabricated 5-nm ZrO2 film, as well as after subsequent vacuum anneals at 940°C, for different times. The first change in the spectra is observed in the synchronous narrowing of the O and Si peaks. This corresponds to the initiation of a non-uniform degradation of the interface SiO2 via the reaction

\[
\text{Si(s)} + \text{SiO}_2(s) \rightarrow 2\text{SiO(g)}.
\]

As interface voids expand laterally, the ZrO2 film, deprived of SiO2 support, comes to direct contact with the Si substrate in the void center, and subsequent decomposition follows reactions (1a) and (1b) with silicide island formation at the center of the expanding voids in the ZrO2 film. In this model, the lateral diffusion of Zr atoms, as suggested in a previous study,2 is not need for silicide nucleation. With increasing annealing time, the height of the Zr peak becomes smaller, without a width change. At the same time, a surface Si peak appears. This is interpreted as the lateral growth of voids in the ZrO2 layer without thinning of the remaining ZrO2 film. The height of the Zr peak is to first approximation

![Figure 1 MEIS energy spectra for a 5-nm ZrO2 film upon annealing for indicated time periods at 940°C](image)
proportional to the surface fraction $\Theta$ covered by zirconia. As shown in the inset to Fig. 1, the decomposition kinetics is accelerating during the initial period of void growth, and slows down in the later stage. The observed behavior is consistent with the rate-limiting reaction taking place at the void edge. The decomposition rate increases while the void circumference becomes larger, and decreases after the voids coalesce and $\text{ZrO}_2$ island shrinking takes place. The final phase of the stack decomposition is dominated by the silicide islands on the clean Si surface. A schematic picture of our decomposition model is presented in Fig. 2.

Since the decomposition reaction originates at the interface, the thermal stability of a high-$\kappa$ stack can be improved by control of the interfacial SiO$_2$ layer. Admitting oxygen gas at low partial pressure causes reoxidation of the SiO(g) decomposition product into SiO$_2$ and therefore thermally stabilizes the stack against decay. Alternatively, a thicker ZrO$_2$ layer will reduce the SiO(g) escape rate into the gas phase. The local concentration of SiO at the interface will rise and therefore will shift the equilibrium of reaction (2) to the left. Therefore, a thicker dielectric stack is expected to be more stable. The deposition of the capping poly-Si overlayer for a gate electrode will have a similar effect on balancing Eq. (2) and will result in suppression of the interfacial SiO$_2$ decomposition. It also prevents the diffusion of the ambient oxygen through a high-$\kappa$ oxide and increasing the amount of interfacial SiO$_2$. However, the presence of a poly-Si cap introduces a Si/ZrO$_2$ interface without an SiO$_2$ spacer. As a result, the decomposition of this system starts at lower temperatures (not shown) compared to that for the uncapped stack. The increase of the decomposition temperature of the SiO$_2$ film with increasing thickness up to a coverage of 10 monolayers has been established in several studies. Thus, the stability of the dielectric stack is expected to be better for a structure with a thicker interfacial SiO$_2$ layer, under the conditions that the thickness of the latter is not too large.

**Figure 2** Schematic diagram of the scenario for ZrO$_2$ high-$\kappa$ dielectric stack decomposition
The second example illustrates the growth of a high-κ dielectric stack on a GaAs substrate. In Fig. 3 we compare the energy spectra obtained from a 4-nm thick Al₂O₃ film fabricated on: (a) the native oxide of GaAs (sample I) and (b) a HF-etched crystal (sample II). In the case of the native oxide terminated substrate, the Ga/As peak intensity is significantly higher, and the O peak is slightly broader. The ratio of the O to Al intensity is found to be 1.7 for the alumina film grown on the native oxide, and the stoichiometric value of 1.5 for that on pre-cleaned surface. These observations confirm the preservation of the GaₓAsᵧO interfacial layer for the first sample and its removal for the HF-etched one. The comparison of the MEIS spectra from HfO₂ films grown on the oxidized and pre-etched GaAs show similar results, in good agreement with TEM images. Using the results of electron energy loss spectroscopy from TEM on the relative content of Ga and As in the interfacial layer, we have been able to establish that the Ga oxides are present mostly in the form of Ga₂O. Upon annealing the sample I at 680°C for 5 min, the O peak width is reduced to that of sample II, indicating interfacial oxide decomposition. However, the Ga/As peak does not decrease to the expected intensity, implying that a disordered GaAs layer remains at the interface.

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References