Extending the Life of N/O Stack Gate Dielectric with Gate Electrode Engineering

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Abstract

Nitride/oxynitride (N/O) stack gate dielectrics show significant leakage reduction and strong boron penetration resistance as compared to oxynitrides. The life of the N/O stack can be further extended by gate electrode engineering. With pre-doped poly-Si gates for both N- and P-MOS devices, poly-Si gate depletion can be minimized and inversion Tox can be reduced. Employment of NiSi can further reduce inversion Tox by minimizing gate dopant deactivation. In addition, a fully-silicided (FUSI) NiSi metal gate electrode totally eliminates poly-Si gate depletion and reduces the inversion Tox by 4-6A. Both FDSOI devices and strained Si devices with N/O stack and FUSI metal gate showed performance improvements and no degradation in gate dielectric reliability.

1. Introduction

The ITRS specifies a continued CMOS scaling in the next decade. This requires an aggressively reduced inversion gate oxide thickness. Although intensive research has been done on high-k gate dielectrics, many difficulties still exist in implementing high-k gate dielectrics for high-performance, thin EOT applications. Among the major problems are mobility degradation and trap-induced threshold voltage shift [1,2]. It is therefore necessary to extend the conventional N/O stack dielectrics [3,4] to the 65nm node and beyond.

This paper reports how to extend life of N/O stack dielectrics by gate electrode engineering, including pre-doped poly gates, employment of NiSi, and FUSI metal gate electrodes. Data reported here includes performance and reliability results from bulk Si, strained-Si and fully-depleted SOI (FDSOI) CMOS devices.

2. N/O Stack Dielectric with Poly Electrode

Fig. 1 shows a SEM cross-section of a 40nm Lgate MOSFET with a gate stack consisting of ultra-thin N/O stack dielectrics, pre-doped poly-Si gates, and NiSi [4]. A TEM cross-section of the ultra-thin N/O stack is shown in Fig.2. The stacked gate dielectrics were formed by thermal growth of oxynitride followed by Si3N4 deposition. The N/O stack gate dielectric showed significant reduction in gate leakage as compared to only oxynitride made using nitrogen containing gases (i.e. N2O, NO). Fig. 3 shows that the direct tunneling leakage current through N/O stack gate dielectric is reduced by more than one order of magnitude, compared to an oxynitride with the same equivalent oxide thickness. For the same gate leakage level, a reduction of ~3A EOT has been achieved with N/O stack.

Due to high nitrogen concentration at the interface between gate dielectric and poly gate electrode, N/O stack films showed very strong resistance to boron penetration (Figs. 4, 5 and 6). This allows minimizing poly depletion by using pre-doped gates for both NMOS and PMOS. Pre-doping the poly gates before gate patterning achieves about 2A inversion Tox reduction (Fig. 7).

The employment of NiSi was also found to reduce inversion Tox due to the lower process temperature for NiSi formation than for CoSi2 formation. The low temperature minimizes dopant deactivation in the poly gates. About 0.8A inversion Tox reduction was achieved with NiSi compared to CoSi2 (Fig.7).

The intrinsic reliability for the ultra-thin N/O stack films with NiSi silicided poly gates was evaluated by the dual voltage TDDW technique [5]. Fig. 8 shows the time-to-failure as a function of stress voltage for the 12A EOT film. A set of I-t curves at a stress voltage of –2.5V and the monitor voltage of –1V is shown in the
3. N/O Stack with Metal Electrode

Inversion Tox can be further reduced by using a metal gate electrode. Metal gate electrodes totally eliminate poly-Si gate depletion. Recently fabricated CMOS devices used N/O stack gate dielectrics and metal gate electrodes [6,7,8]. Here, the metal gate electrodes were realized by an easily integrated full silicidation of poly gates. NiSi was chosen because of its good scalability, low process temperature, low stress, and good compatibility with SiGe. Compatibility with SiGe is important for fabricating strained-Si channel devices [8,9]. The workfunction of NiSi can be tuned by doping engineering [7,10].

Fig. 9 shows our FUSI process flow. CMP was used to expose the top of poly gates after the ILD layer deposition. An additional silicidation step was used to fully silicid the poly gates. The flow is relatively simple compared to other metal gate integration approaches.

Figs. 10, 11 and 12 show TEM cross-sections of a 25nm Lgate FDSOI MOSFET and a 35nm Lgate strained-Si NMOS devices, both of which have N/O stack gate dielectric and NiSi FUSI metal gate electrodes. A TEM of the 16A N/O stack sandwiched between strained-Si and NiSi is shown in Fig.13. Fig.14 shows a high frequency CV curve of a NMOS capacitor with the 16A N/O stack gate dielectrics and NiSi metal gate. CV curves of strained-Si and unstrained-Si NMOS capacitors with poly gates are also shown in Fig. 14 for comparison. About 5A reduction in inversion Tox at 1.2V has been achieved through elimination of poly gate depletion. Fig. 15 shows the CV curves for a pair of FDSOI CMOS capacitors with an ultra-thin (~13A) N/O stack gate dielectric and a NiSi metal gate electrode. This achieves ~16A inversion Tox at 1.2 Vdd. Again, the NiSi gate electrode reduces inversion Tox by ~5A.

Fig. 16 shows measured electron mobility from long channel NMOS devices. No mobility degradation was observed with NiSi metal gate. A slight improvement in low field mobility was observed with NiSi metal gate. This is believed to be due to the effect of strain induced by NiSi metal gate.

Fig. 17 shows the gate leakage current of the N/O stack gate dielectric with NiSi metal gate electrode is lower than poly gate control devices -- even though the metal gate device has a thinner inversion Tox. The gate dielectric integrity of NiSi metal gate devices was also evaluated by TDDB and negative bias temperature instability (NBTI). Fig. 12 shows NiSi metal gate devices exhibited comparable TDDB characteristics as compared to control devices. The NBTI lifetime projection indicates good immunity to degradation for the FDSOI PMOSFET with 13A N/O stack and NiSi metal gate (Fig.19).

For strained-Si devices, ~25% Idsat improvement is achieved with NiSi metal gates (Figs. 20 and 21), due to elimination of poly-Si gate depletion. In the case of FDSOI devices, NiSi metal gate induced strain results in an additional device performance improvement, especially for narrow devices (Fig. 22).

4. Conclusions

The life of the N/O stack can be further extended by gate electrode engineering. With predoped poly-Si gates for both N- and P-MOS devices, poly-Si gate depletion can be minimized and inversion Tox can be reduced. Employment of NiSi can further reduce inversion Tox by minimizing gate dopant deactivation. NiSi FUSI metal gate electrode totally eliminates poly-Si gate depletion and reduces the inversion Tox by 4-6A. Both FDSOI devices and strained Si devices with N/O stack and NiSi metal gate showed performance improvements and no degradation in gate dielectric reliability.

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References
Fig.1 40nm N-MOSFET with N/O stack dielectric, pre-doped poly gate, and Ni salicide.

Fig.2 TEM cross-section of 9A EOT N/O stack gate dielectric.

Fig.3 NMOS capacitor gate leakage current (@Vg=1.2V) vs. gate dielectric EOT.

Fig.4 Vt shift vs. RTA time for PMOS capacitors

Fig.5 CV curves of PMOS capacitors with different RTA times, showing significant reduction of boron penetration induced flat band shift with N/O stack

Fig.6 IV curves of PMOS capacitors with different RTA times, showing significant reduction of boron penetration induced leakage with N/O stack
Fig. 7 Inversion Tox reduction with poly gate doping and silicide engineering.

Fig. 8 Time-to-failure as a function of stress voltage for 12A EOT N/O stack films. Time-to-failure is determined by TDDW tests.

Fig. 9 Process flow for Full Silicidation (FUSI) of poly-Si gate.

Fig. 10 TEM cross-section of a 25nm Lgate FDSOI MOSFET with a N/O stack gate dielectric and a FUSI NiSi metal gate electrode.

Fig. 11 TEM cross-section of a 35nm Lgate strained Si NMOS transistor with NiSi FUSI gate electrode.

Fig. 12 STEM cross-sectional image, clearly showing fully silicided gate and strained Si layer.
Fig. 13 High resolution TEM cross-sectional image of 1.6nm N/O stack sandwiched between strained-Si and NiSi.

Fig. 14 High frequency CV curves of NMOS capacitors.

Fig. 15 CV curves of a pair of FDSOI CMOS capacitors with 13A N/O stack and NiSi metal gate

Fig. 16 Channel electron mobility measured from long channel NMOS transistors

Fig. 17 Gate leakage current density as function of gate bias.

Fig. 18 TDDB for NiSi FUSI gate strained Si (circle) and poly gate strained Si (square) NMOS capacitors.
Fig. 19 NBTI lifetime projection for a FDSOI PMOSFET with 13A N/O stack and NiSi metal gate.

Fig. 20 Ids-Vds of 35nm NiSi FUSI gate strained Si (a) and poly gate strained Si (b) NMOS, in comparison with poly gate unstrained Si device (dash line).

Fig. 21 Percentage saturation drive current enhancement for NiSi FUSI gate and poly gate strained Si devices.

Fig. 22 Percentage saturation drive current enhancement for NiSi FUSI gate and poly gate strained Si devices.